

Custom DAQ Module for Timing and Energy Measurements for J-Parc E14

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Abstract—We present a Pulse Shaping/Data Processing ADC Module for timing and energy measurements in High Energy Physics Experiments. The 6U VME Board has 16 channels at 14-BIT, 125MSPS, and was originally designed for KOTO, a Kaon experiment at Japan Particle Accelerator Research Complex (JPARC). Before being digitized, the differential inputs are amplified and shaped with low-pass filters, designed specifically for the scintillating material used in the experiment. Following shaping and sampling, data are fed to the on-board FPGA, and stored inside an adjustable pipeline memory, awaiting the trigger pulse. A digital data delay of up to 5,000 samples is possible. The Module can work independently, in a self-trigger mode, or it can be part of a large DAQ system with a unique system trigger. For sampling, the Module can use a locally generated clock, or it can work on a system level, simultaneous clock, provided at its front panel. After trigger, sets of data are packed and buffered. Depending on throughput requirements, the readout can be performed via the VME64 back plane or via the front-panel optical links. The powerful processing capabilities within the high-density FPGA allow for future design enhancements. Real-time local data processing and reduction algorithms can be implemented. The Module is fitted with two optical link transceivers at the front panel with 2.5 GBPS each. One optical link output is used for data read-out, and one for real-time total energy values. The two optical-link inputs are used to merge energy values calculated in other modules. By doing this, one can successively calculate the energy for the entire system and generate Level 1 triggers, with no additional hardware required. Design, module specifications, and test results will be described.

I. INTRODUCTION

THIS paper presents a custom DAQ Module designed for the Step-1 phase of KOTO [1], a high energy physics kaon experiment at the Japan Particle Accelerator Research Complex (J-PARC). The goal of KOTO is to measure the rate of the rare decay $KL \rightarrow \pi^0 \nu \nu$, predicted by the Standard Model to happen only once every 3.3×10^{11} KL decays. The Experiment plans to shed light on the mechanism responsible for CP in the quark sector.

The 16-Channel DAQ Module was designed to be used for both timing and energy measurements, as well as for real-time data processing. The Module is also provided with two optical link inputs, which allow it to process and merge information received from other similar modules in the detector. With this feature, the Module can be used for energy calculation at the crate and system level, and for Level 1 trigger generation.

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II. ARCHITECTURE

The DAQ Modules are distributed 16 per one 6U VME Crate, and receive analog pulses directly from the PMTs. There are two distinctive board flavors:

- Cesium Iodide (CsI) boards, each reading out 16 of ~3000 crystals in the KOTO CsI calorimeter.
- Veto Detector boards, the same custom modules, fitted with a different firmware, for the readout of ~700 channels.

The Module's block diagram is presented in Figure 1. There are three main blocks. The signal conditioning and conversion block, the data processing block, and the interface block.

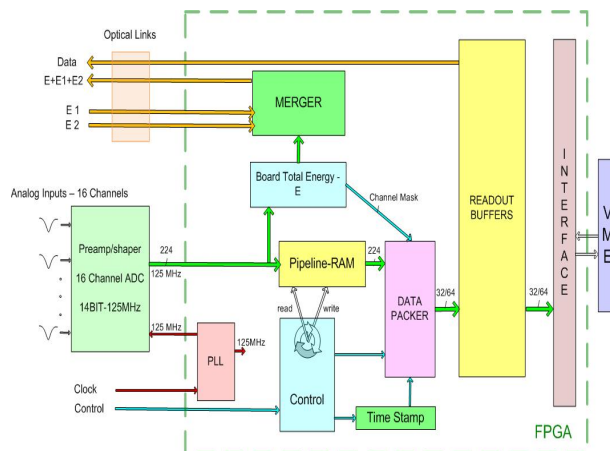


Fig. 1. Block Diagram of a custom 16-Channel DAQ Module.

A. Signal Conditioning and Conversion Block

In the CsI Calorimeter, every analog pulse generated by the photomultiplier tube (PMT) is amplified and passed through a 10-pole filter/shaper with a cutoff frequency of about 10 MHz, which converts the fast PMT pulse into a Gaussian form, while keeping the total energy information constant. The filter/shaper was calculated for optimal Full Width Half-Height (FWHH) of the resulting shape with respect to fitting and timing. After shaping, each pulse is applied to a sample-and-hold ADC chip (AD9254). By performing a fit of the output shape with a fixed width Gaussian function, one obtains two key parameters: the height of the Gaussian, which measures the total charge (energy) of the pulse, and the position of the peak, which measures its timing.

Sampling for all calorimeter channels is simultaneous, on a low jitter System Clock. For testing purposes, each board can switch to a locally generated 125 MHz clock.

B. Data Processing Block

Digitized data are processed locally with Field Programmable Gate Arrays (FPGAs), Altera EP2S60F1020C5 chips from the STRATIX II family [2] that perform the board total energy calculation and determine real-time board energy related values. These values are merged with energy levels calculated by other two boards and passed further, via 2.5Gbps Optical Links, for a system-wise energy calculation and eventual Level 1 trigger pulse generation.

Each ADC module is provided with a pipeline, over 4 μ s (5,000 samples) long, which stores the acquisitions while awaiting the system trigger pulse. After a trigger, data are packed and buffered for readout. Depending on the volume of data, readout is performed via the 2nd front panel Optical Link, or via the VME64x backplane.

C. Interface Block

The Module is provided with two optical link transmitter, two optical link receivers, and four LVDS connection, all on the front panel. In the current configuration, the links are serviced by TI TLK2501 transceivers and run at 2.5Gbps. Data rates as high as 3.125Gbps are possible with different transceivers on the same PCB. The two optical link inputs and one output are intended for Et sum merging and transmission in the KOTO Experiment. The remaining optical link output is intended for data readout.

In the KOTO Experiment we intend to record 64 samples for each trigger, spread over a 512 ns period. Since all samples are held in a pipeline memory in wait for the trigger, the recording has to be precisely synchronized with the trigger moment, and to account for the actual delay required to generate it. Considering a data bandwidth of 2Gbps for the output link, and a channel hit occupancy of 10%, the resulting supported trigger rate is in excess of 1 MHz.

All optical links lead to the local FPGA, so their functionalities are configurable to serve different purposes for different work modes on the same experiment, or for completely different implementations. For example, the output normally used for Et sum, can be used to transmit any one ADC channel raw data recordings, in a continuous, trigger less mode. This feature may prove useful in the commissioning phase of the experiment.

III. SPECIFICATIONS

Figure 2 presents one of the prototypes that was built and tested. Some of the main specifications are as follows:

- 6U VME64x standard;
- 16-channels, 14BIT ADC;
- Max 150 MHz sampling rate;
- Differential or single ended inputs;
- Configurable gain and signal offset;
- Up to 10-pole low pass filter/shaper – configurable;
- SNR \sim 74dB (noise STDEV \sim 1.90LSB);
- Digital I/Os: 3 LVDS inputs, 1LVDS output;
- 2 Optical Link inputs, 2 Optical Link outputs.

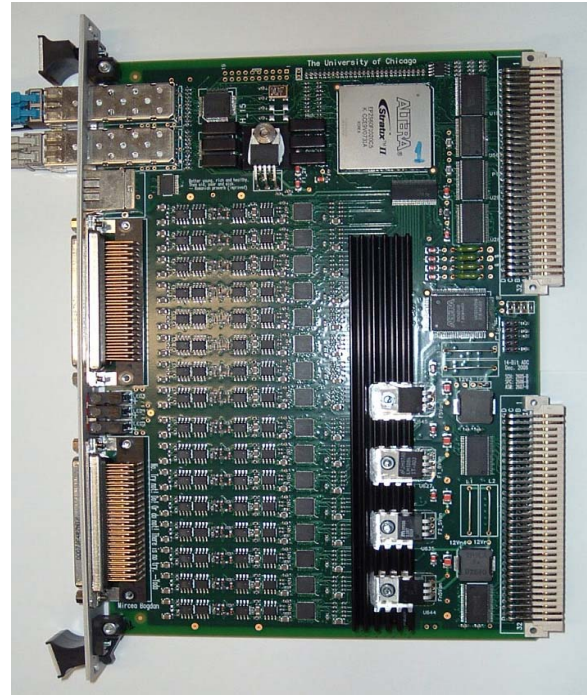


Fig. 2. Prototype DAQ Module.

IV. TRIGGER

Figure 3 illustrates the way this Module can be used to merge data, and to calculate crate-level and system-level total energy values. The basic idea is to use the two optical link inputs to receive Et sums from two upstream Modules and add them to the locally generated Et sum. By doing this, three Et sums are merged together, representing the energy from 48 analog channels.

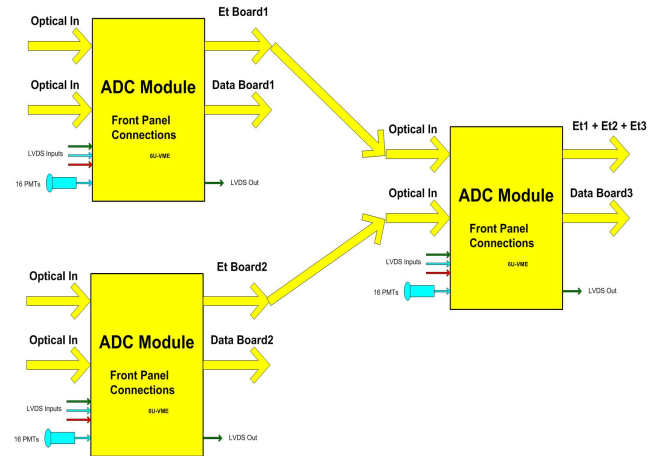


Fig. 3. Configuration used to generate Et sum for 3 DAQ Modules, i.e. 48 analog channels.

Figure 4 presents one way to use the DAQ Modules for a crate-wise total energy calculation. The Modules can be connected in a pyramid scheme, as illustrated, or in any other type of configuration (e.g. a daisy-chain structure). It takes less than 100 clock cycles, 800ns, to generate Et sum for all the 15 Modules, as connected.

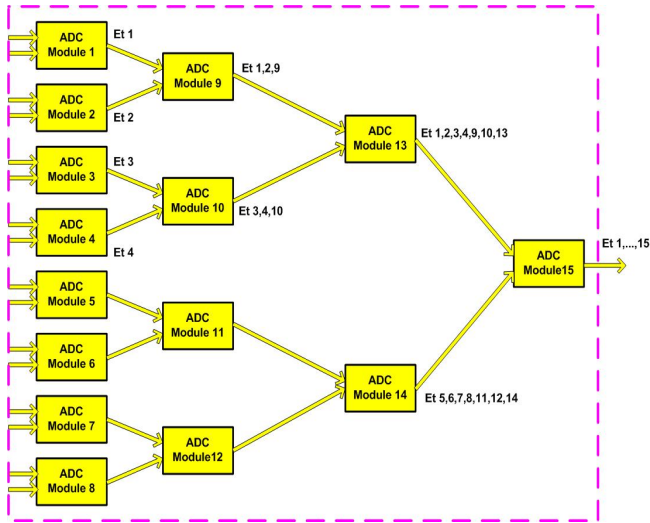


Fig. 4. Configuration used to generate Et sum for 15 DAQ Modules, i.e. 240 analog channels. Only the Et sum related connections are represented.

Figure 5 presents one way to use the DAQ Module for a system-wise total energy calculation. This example configuration can be used to generate Et sum for 255 DAQ Modules, i.e. 4080 analog channels.

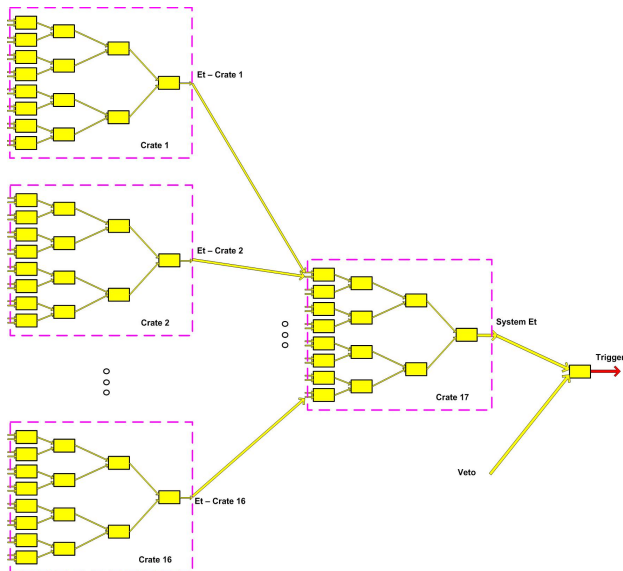


Fig. 5. Configuration used to generate Et sum for 255 DAQ Modules, i.e. 4080 analog channels. Only the Et sum related connections are represented.

As connected, it takes about 250 clock cycles to generate a Level 1 trigger pulse. The pipeline memories inside the FPGAs can accommodate more than 5,000 clock cycles delay.

Since we have only optical link connections between all the modules in the system, there is no actual proximity requirement. The modules don't have to be adjacent in order to connect in the pyramid scheme. More than that, any other connection scheme can be imagined and implemented. In the

KOTO Experiment we will have about 3,000 channels for the CsI calorimeter.

A similar scheme has to be implemented for the 700 ADC channels in the Veto part of the Detector, and generate the Veto related values. One additional Module, fitted with a different firmware can act as System Trigger Supervisor. This Module can include the Veto and generate the Level 1 Trigger pulses. These pulses can be sent back to the entire system using commercially off-the-shelf fan-out boards.

As described, the system architecture will use three different custom modules: the CsI modules, the veto modules, and the Trigger Supervisor. All modules will have the same hardware, programmed with different FPGA designs.

V. CONCLUSIONS

This is a 16-Channel, 14-BIT, 125MHz, DAQ Module which has some important features:

- It can be used for both energy and timing measurements of narrow PMT pulses. The Module does a signal shaping followed by digital conversion.
- It is very flexible: the Module can be tailored for a different application by changing the 10-pole shaper, and the processing algorithm.
- The Module can merge information received from two other locations and build an architecture producing detector-wise Et sums.
- It can be used as a System Trigger Supervisor. The same Module, provided with different firmware can merge and corroborate the detector-wise Et sums with the Veto values and generate Level 1 triggers.

Using this Module, one can design and build an entire DAQ/Trigger System with no other custom hardware.

REFERENCES

- [1] E14: Proposal for $K_L^0 \rightarrow \pi^0 \nu \bar{\nu}$ Experiment at JParc, approved July 2007.
- [2] Altera Corporation, Stratix II Device Handbook, v.4.4., Jan. 2008.