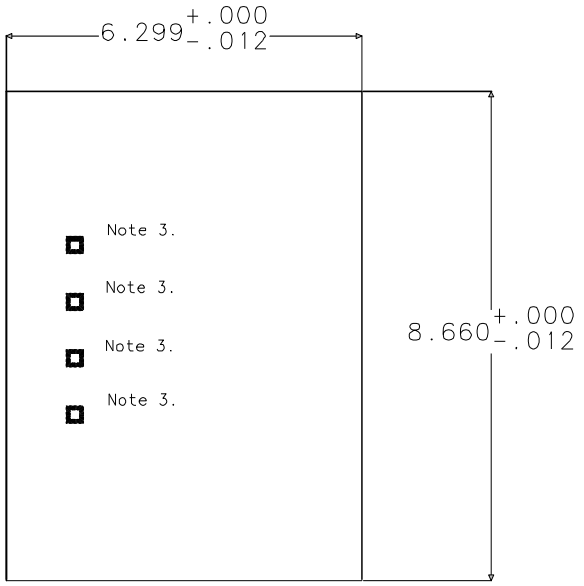

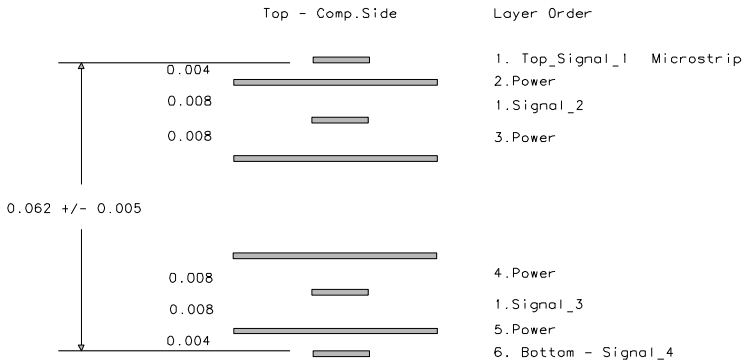

Board Characteristics - 8 LAYER BOARD

1. All dimensions are given in inches unless specified otherwise.
2. Material FR4 Tg> 170C.
3. General trace width/clearence on all layers is 5 mils.
   Special trace width/clearence of 2.5/2.8 mils in 4 small areas on top layer only.
   These 4 small areas are 0.15"x0.15" each.
4. 1/2 oz copper for all layers.
5. Immersion Gold over copper, with min. Ni: 2.5-5 um; Au: 0.05-0.2 um.
6. Apply Solder Mask over bare copper.
8. Silkscreen on Component and Solder Sides.
10. FHS tolerances: +/- 0.003 unless specified otherwise.
11. Interlayer spacing as specified
12. Impedance control: 55 Ohm +/- 10% on all 5 mil traces, inner and outer layers.

BOARD's DRILL SCHEDULE

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Tolerance	COMMENT
○	.008	1295	YES	---	
⊞	.015748031	9	YES	---	
⊕	.035	8	YES	---	
⊟	.041	69	YES	---	
⊖	.042	20	YES	---	
◫	.057	8	YES	---	
⊕	.098425197	2	YES	---	
□	.104	2	YES	---	
	.106	1	NO	---	
	.15	3	NO	---	
	.2	2	YES	---	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX
.XXX
DO NOT SCALE DRAWING

TREATMENT

FINISH

SIMILAR TO | ACT. WT | CALC WT

CONTRACT NO.

APPROVALS	DATE
DRAWN M.Bogdan	8/19/2010
CHECKED M.Bogdan	8/19/2010
ISSUED	

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE: PSEC2 Flip Chip ADC Module Specification Drawing

SIZE | FSCM NO. | DWG. NO. 2708 | REV. A

SCALE 1/2 | SHEET

THIS SHEET IS COMPUTER GENERATED