

4

3

DWG. NO. 2711

SH

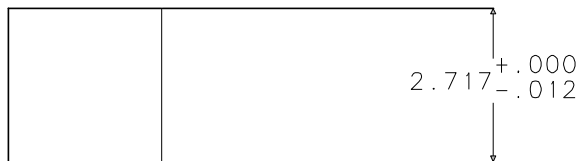
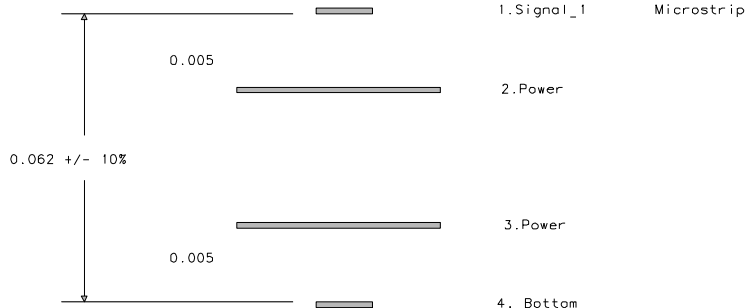
REV. A

1

D

Top - Comp.Side

Layer Order


 $2.717^{+.000}_{-.012}$
 $2.717^{+.000}_{-.012}$


1.Signal_1 Microstrip
2.Power
3.Power
4. Bottom

C

C

Board Characteristics - 4 LAYER BOARD

0. All dimensions are given in inches unless specified otherwise.
1. Material FR4 , Tg > 170 C.
2. Minimum trace width and clearance: 0.006"
3. Impedance control: 50 Ohm for all 6 mil signal traces
4. 1 oz copper for all layers.
5. Immersion Gold over copper, with min. Ni: 2.5-5 um; Au: 0.05-0.2 um.
6. Apply Solder Mask over bare copper.
8. Silkscreen on Component and Solder Sides.
10. FHS tolerances: +/- 0.003 unless specified otherwise.
11. Interlayer spacing as specified

B

B

BOARD'S DRILL SCHEDULE

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Tolerance	COMMENT
○	.013	10	YES	---	
⊞	.014	270	YES	---	
⊘	.032	20	YES	---	
⊞	.041	10	YES	---	
⊖	.094	1	NO	---	
⊞	.106	4	NO	---	

A

A

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX XXX DB. NO.1 SCALE DRAWING	CONTRACT NO.		UNIVERSITY OF CHICAGO ELECTRONICS DEVELOPMENT GROUP		
	APPROVALS	DATE	TITLE		
TREATMENT	DRAWN M. Bogdan	2/15/2011	PSEC3 - QFP Mezzanine Specification Drawing		
FINISH	CHECKED M. Bogdan	2/15/2011	SIZE	FSCN NO.	DWG. NO. 2726
SIMILAR TO	ACT. WT	CALC. WT	ISSUED		REV. A
			SCALE 1/2	SHEET	

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2

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