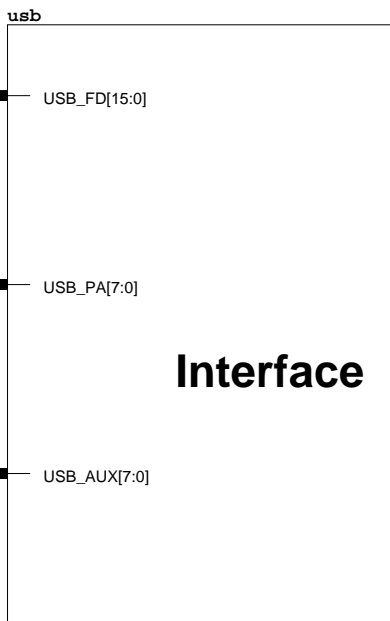
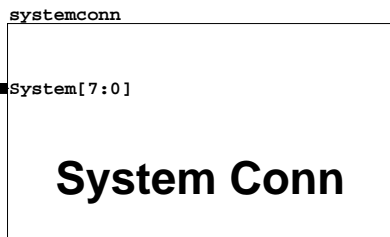
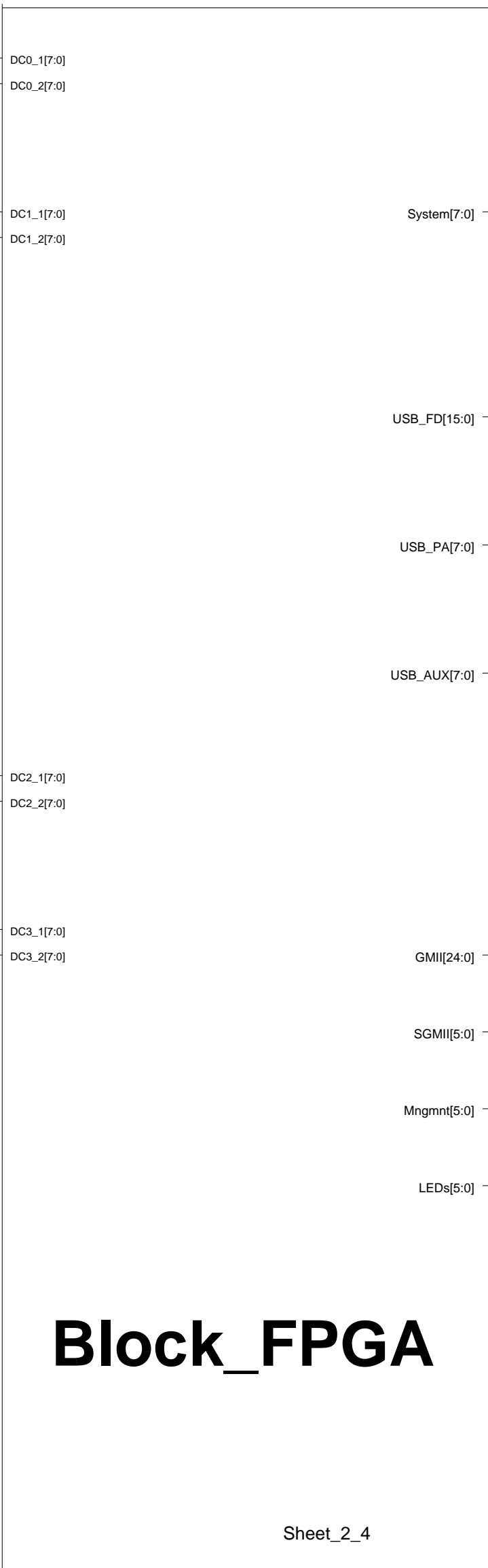
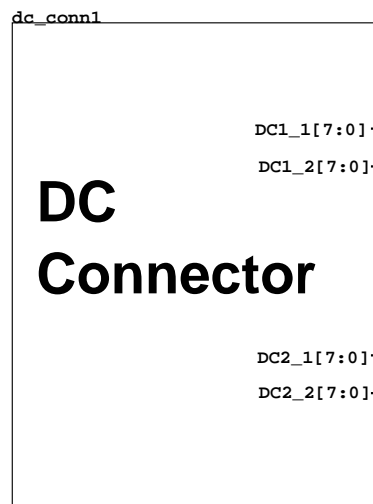


D

D

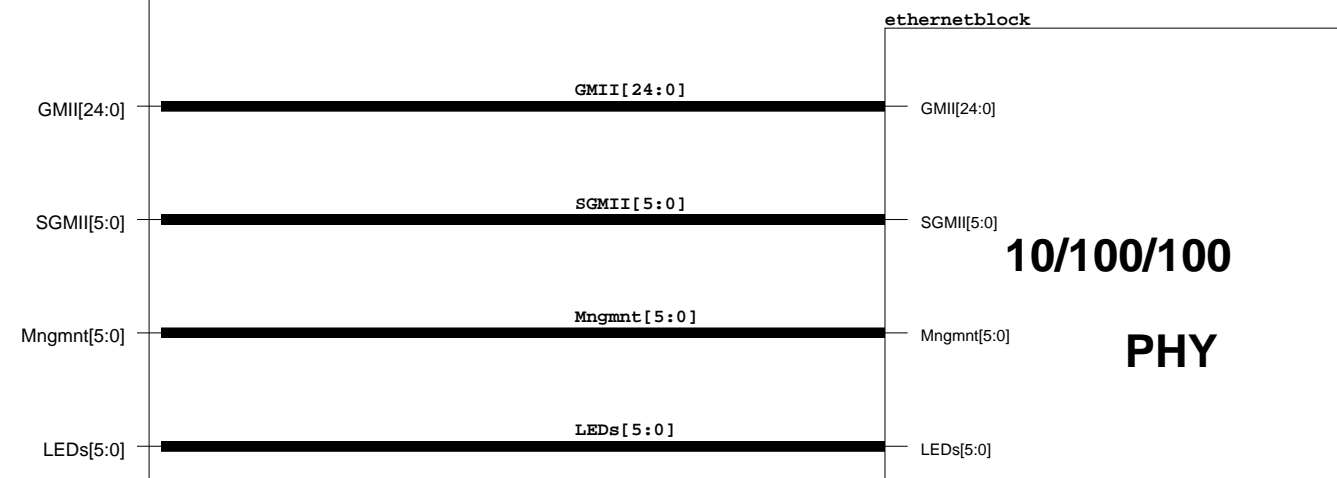
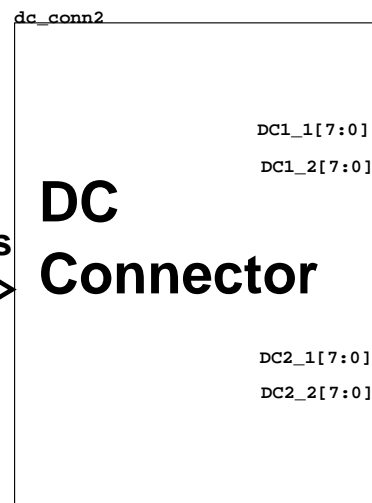
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Left Side →



C

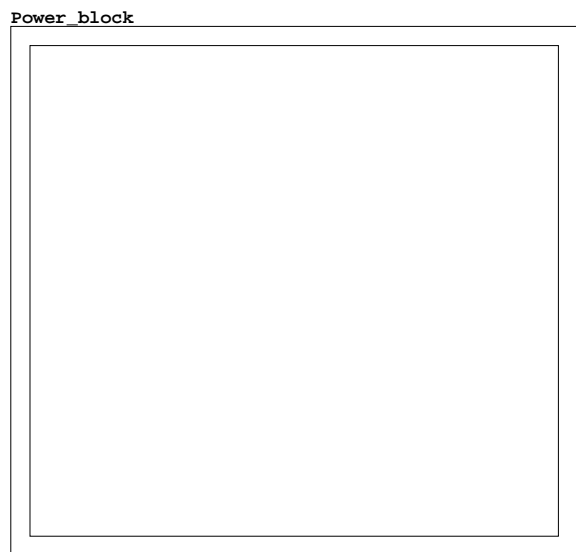
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To/From Digital Cards  
Right Side →



B

B



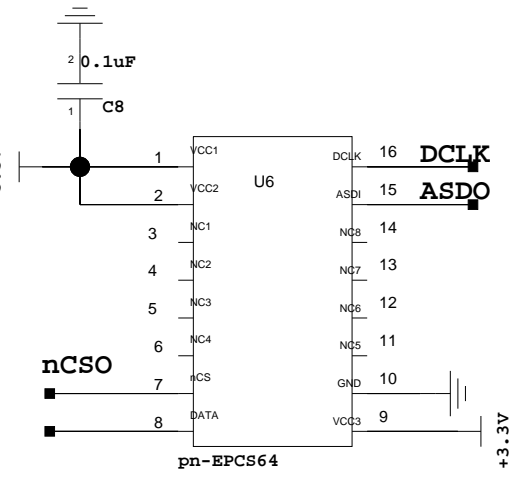
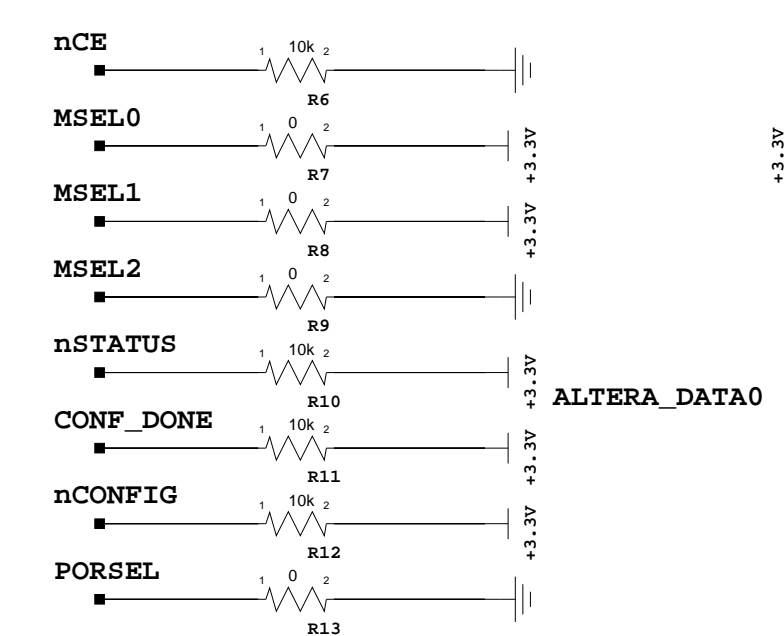
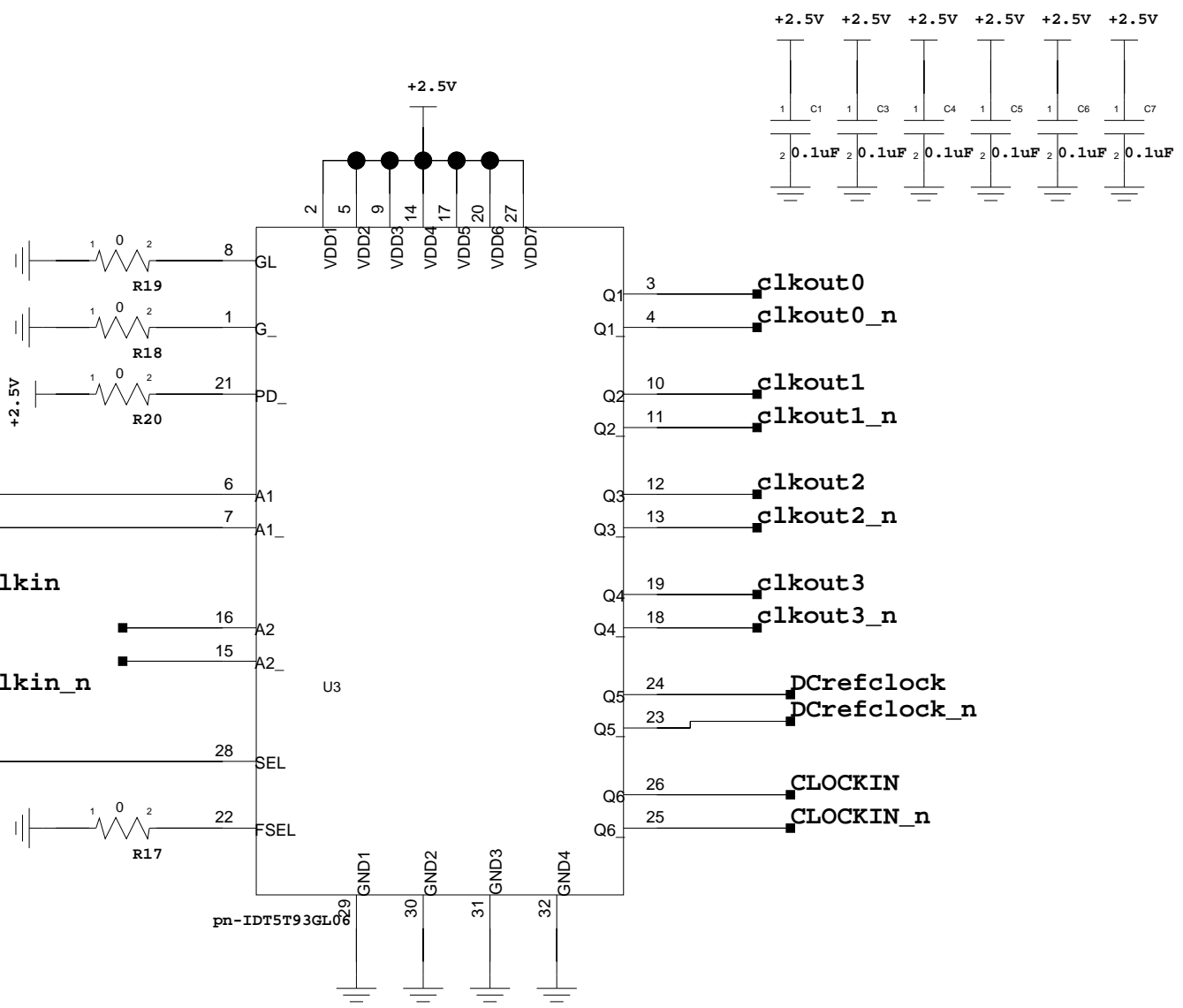
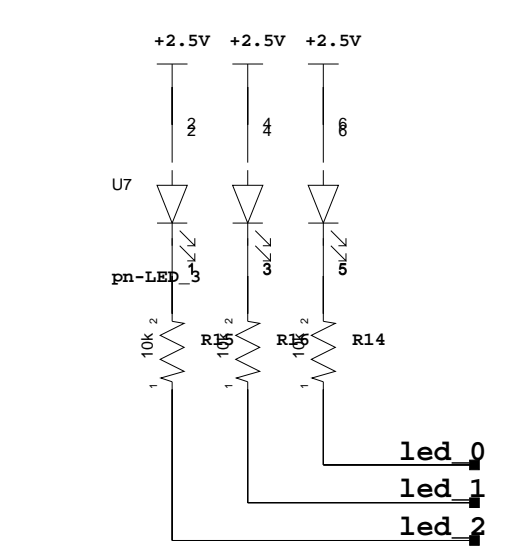
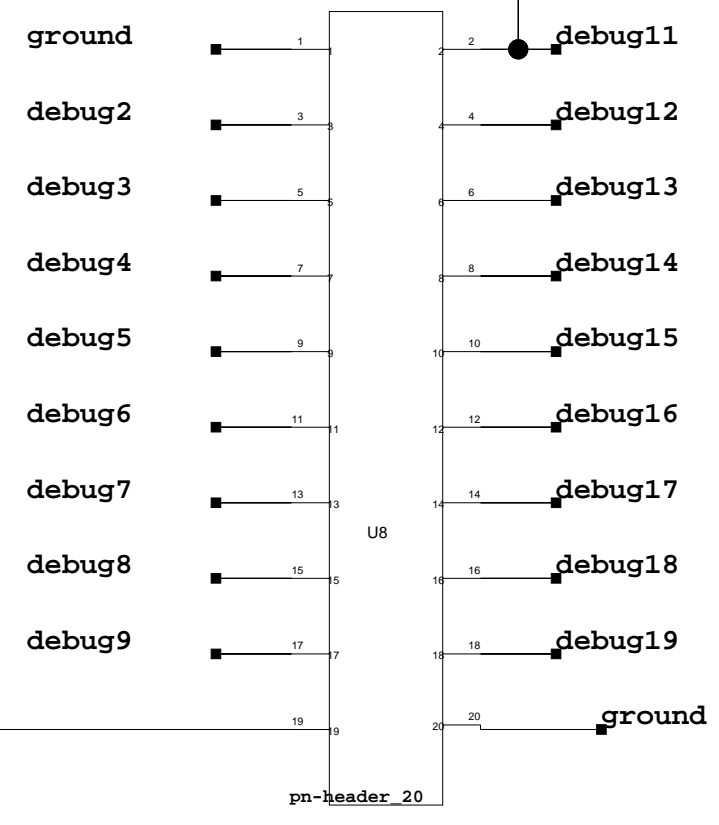
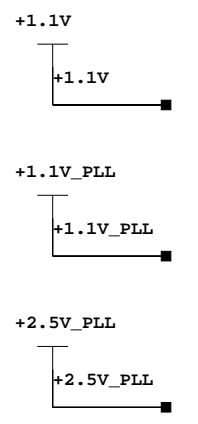
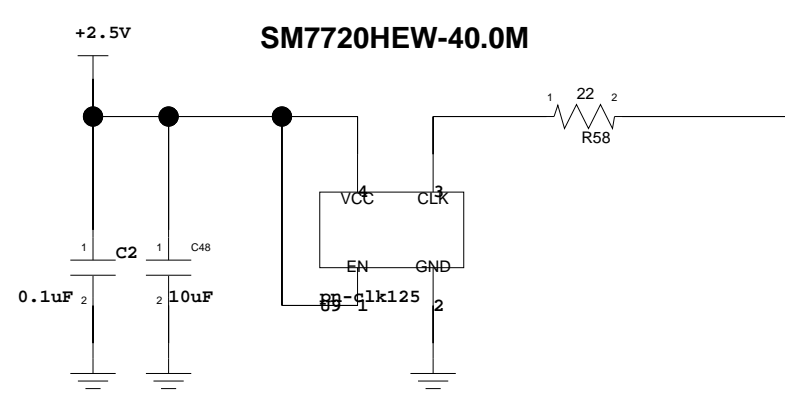
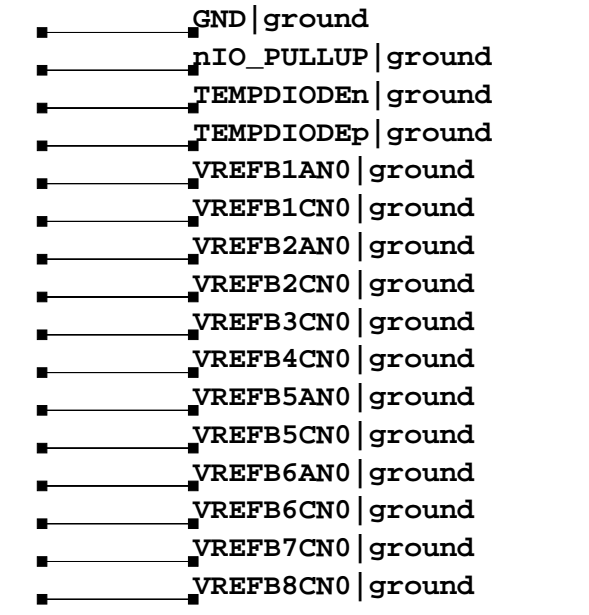
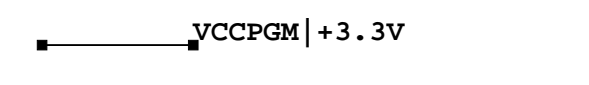
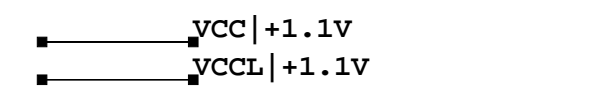
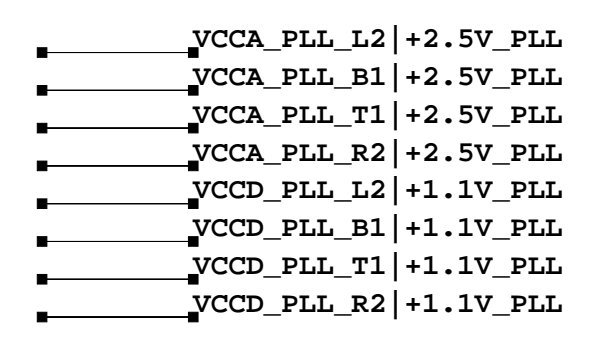
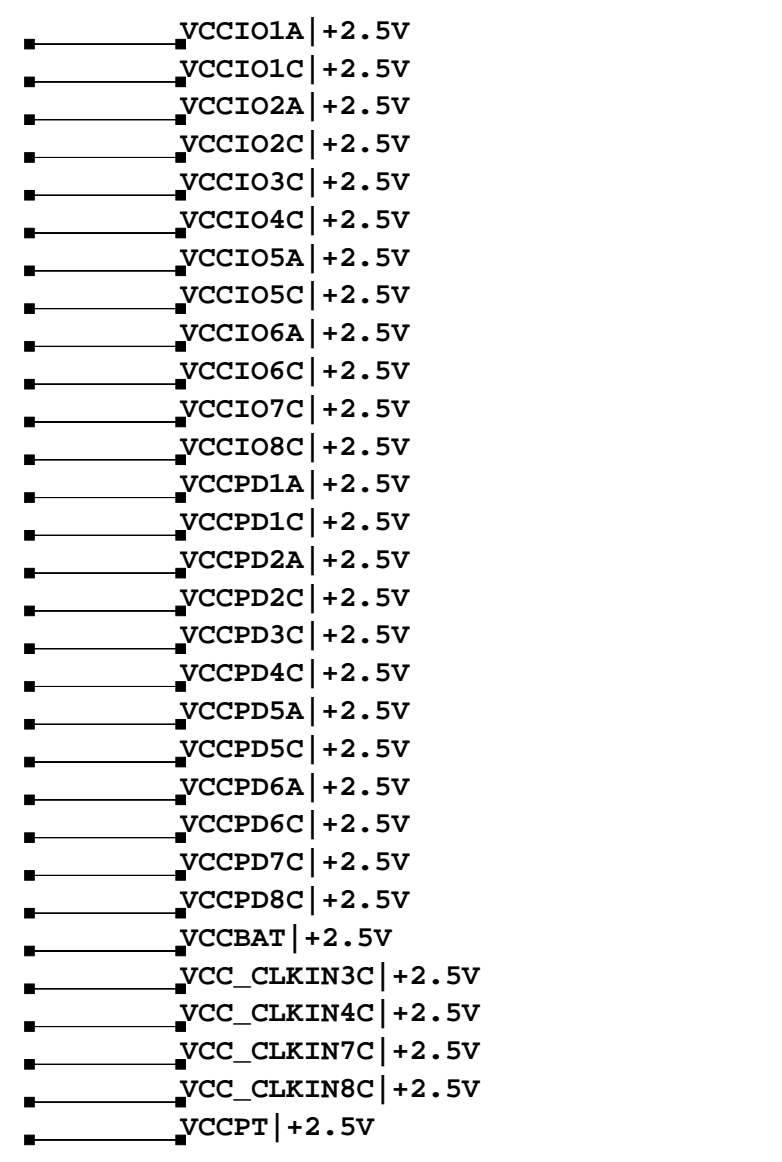
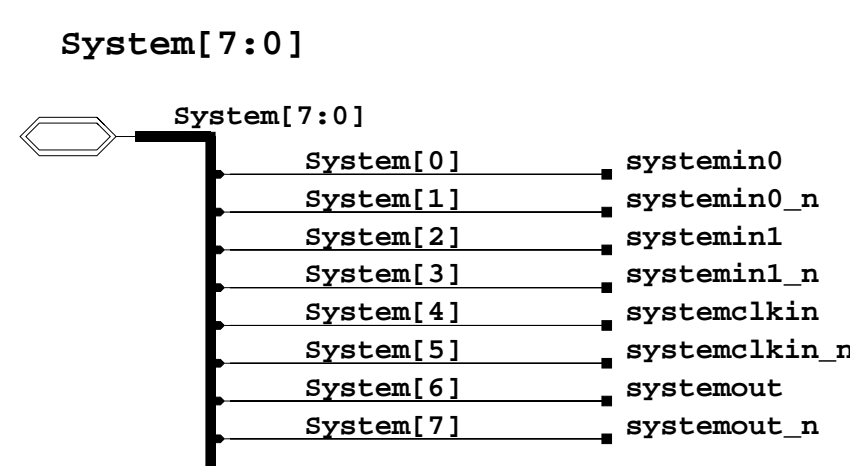
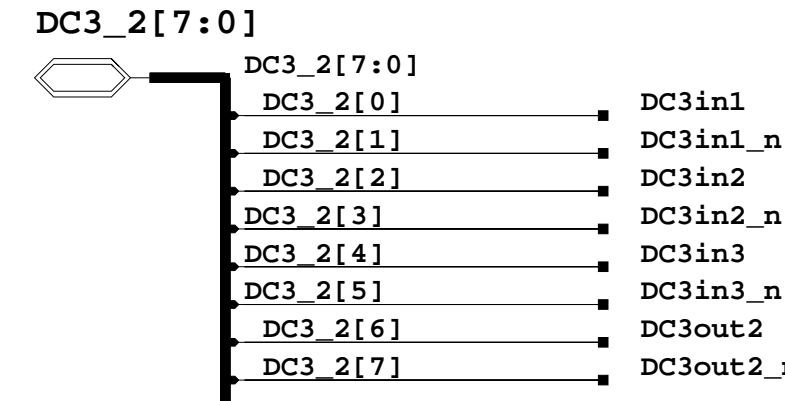
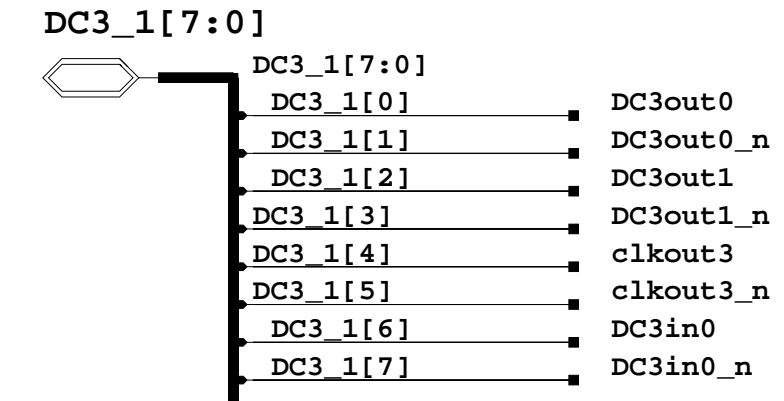
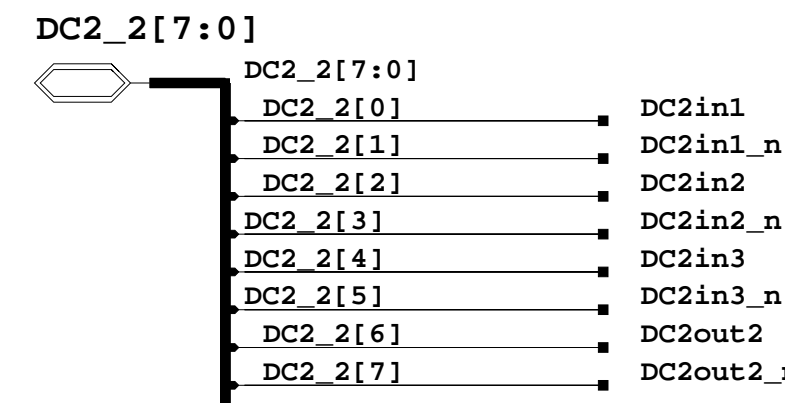
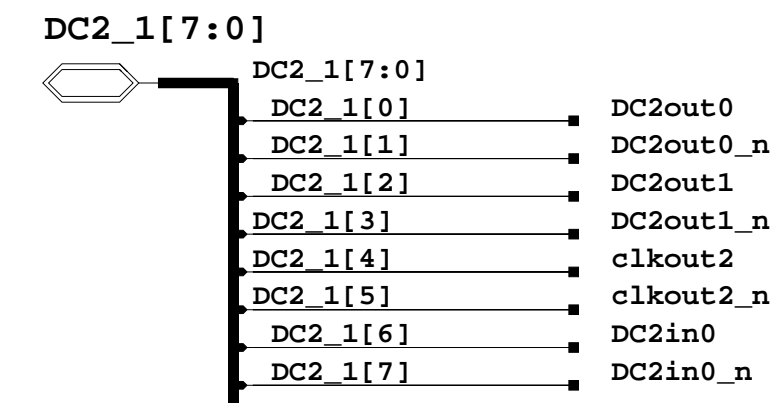
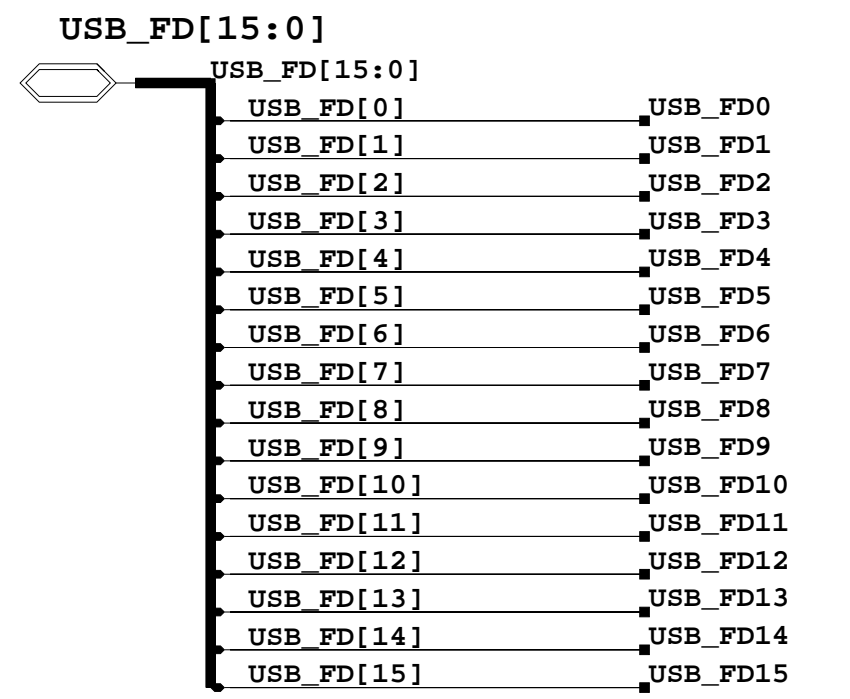
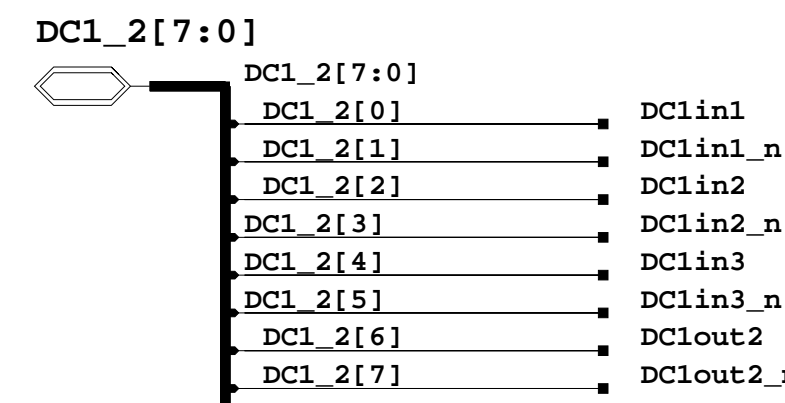
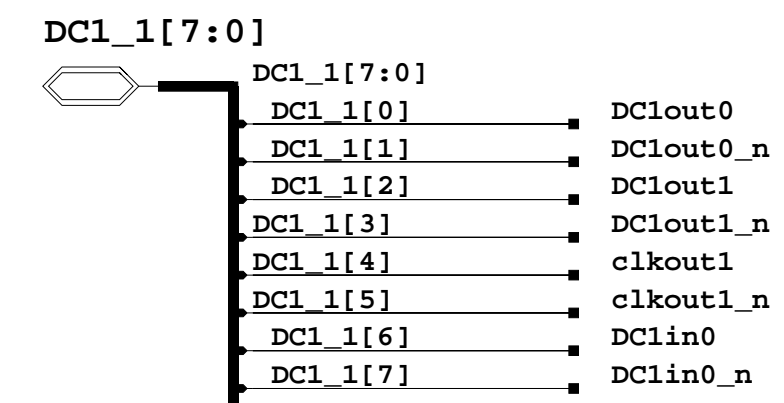
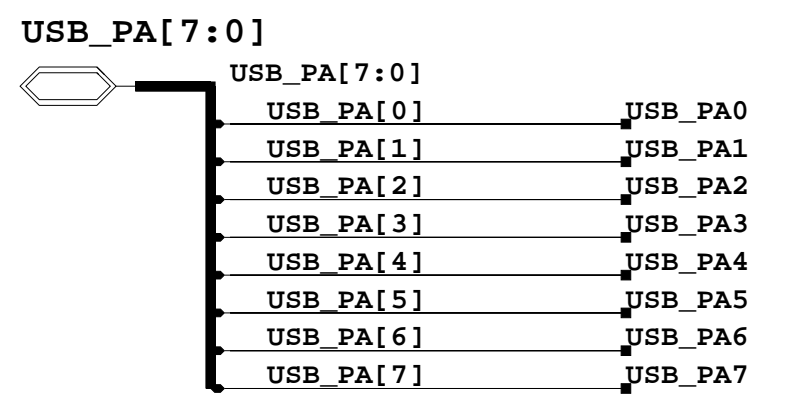
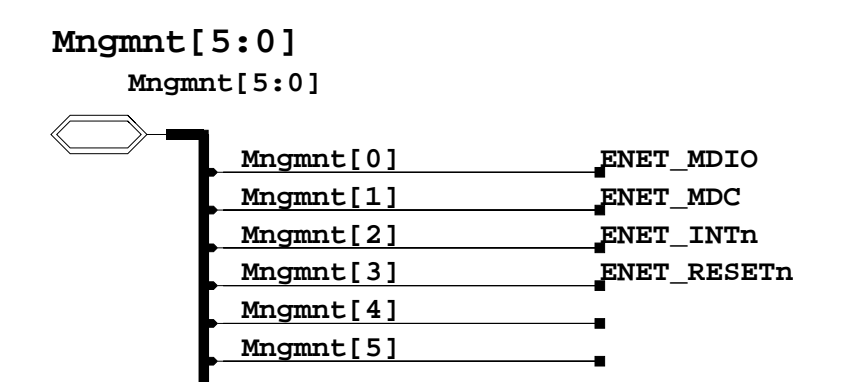
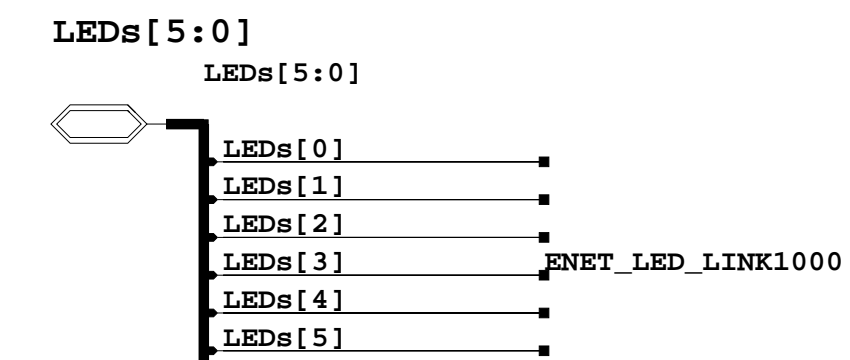
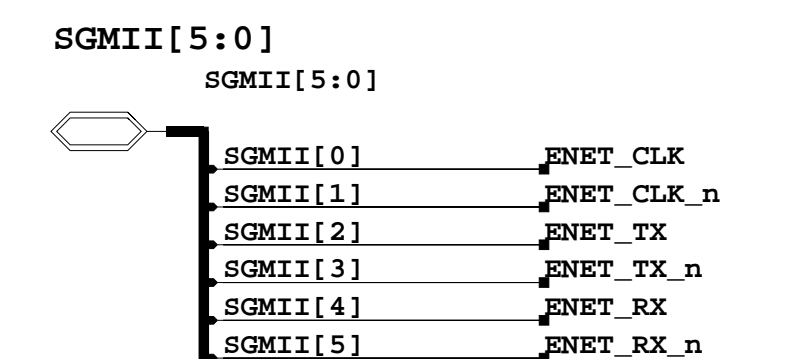
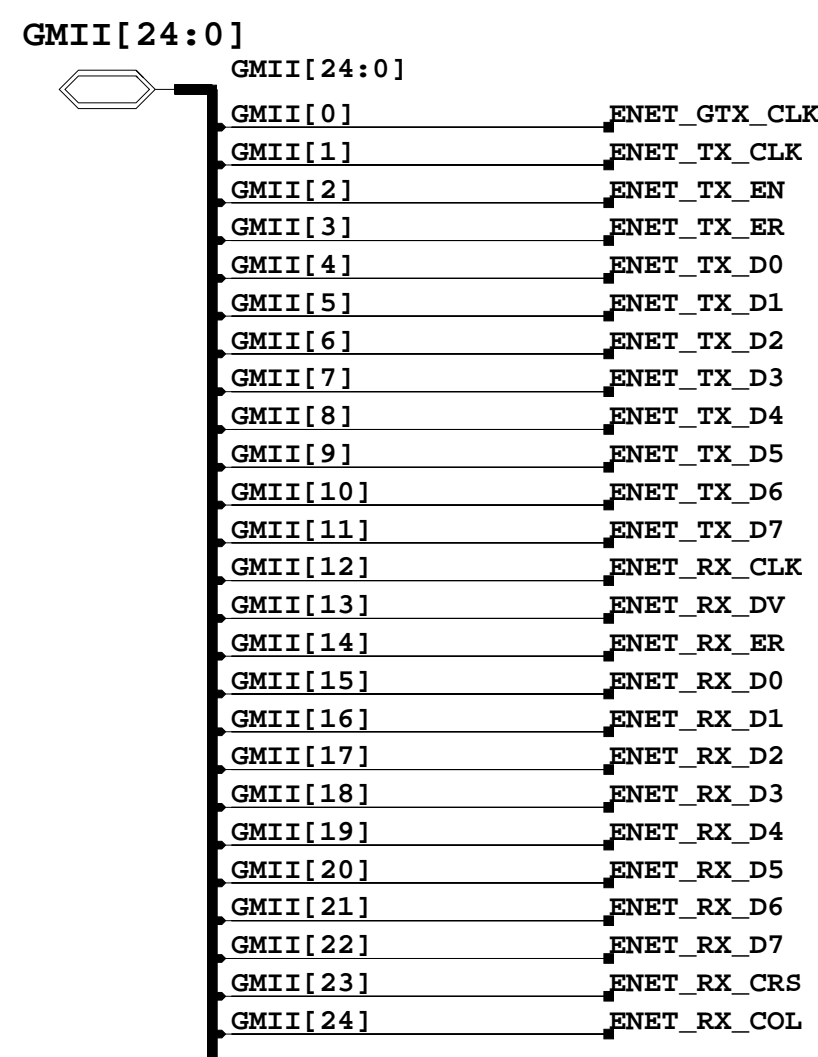
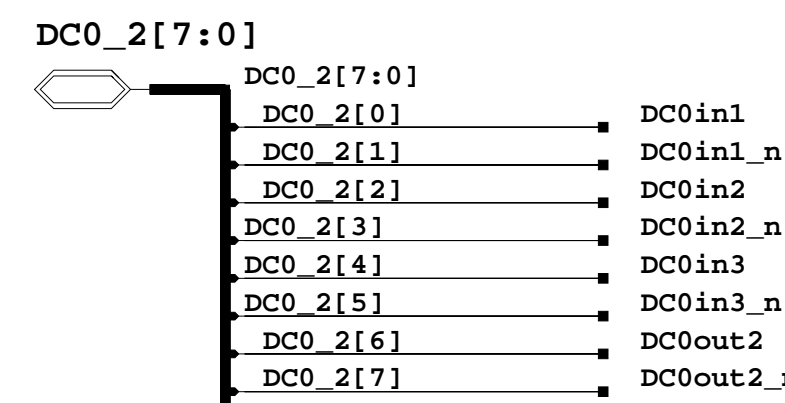
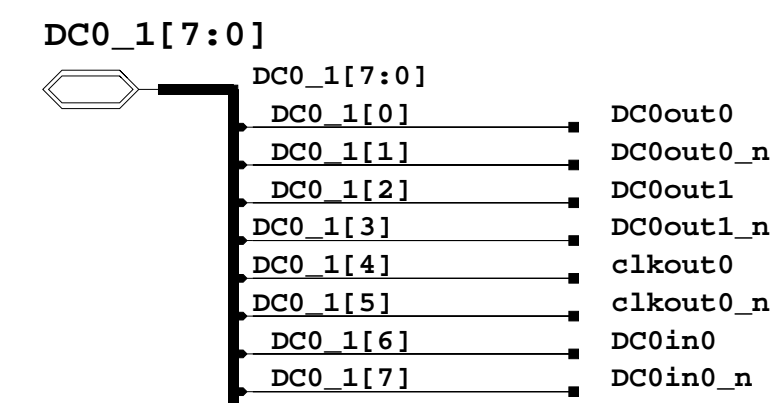
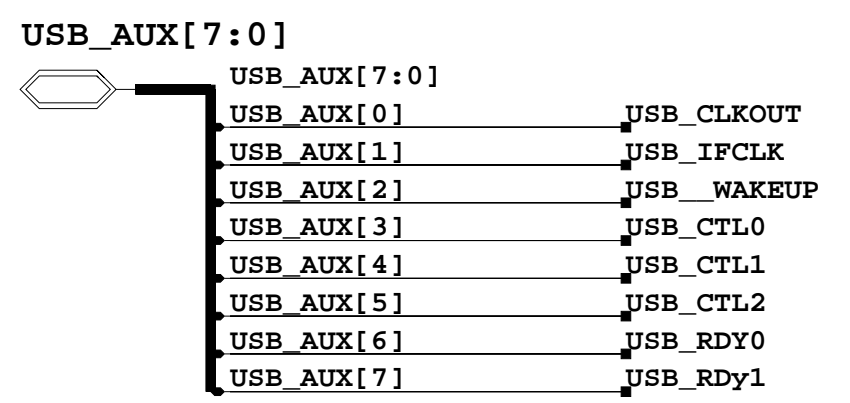
A

A

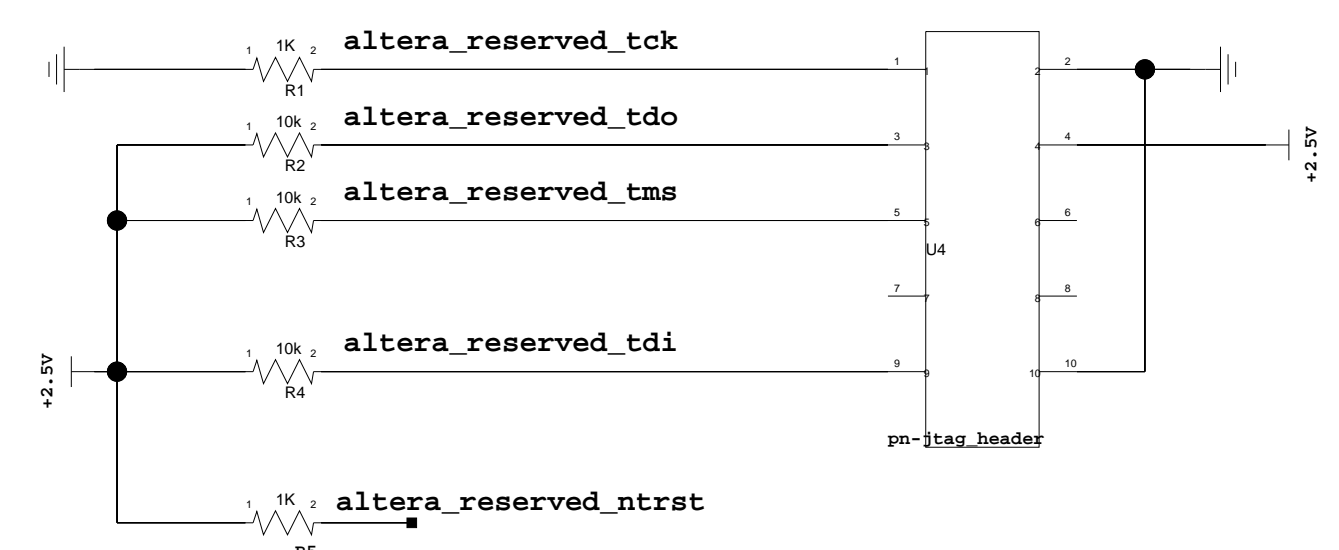
Sheet\_2\_4

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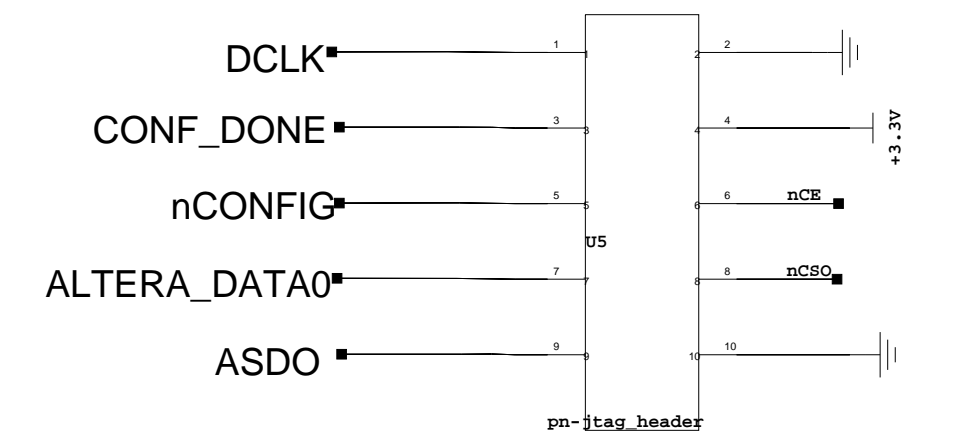
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SIZE				2766 Rev. A	
C		DWG NO		REV 0	
SCALE		SHEET		of 1/7	
DRAWN BY				06-01-2012_12:08	
Mircea Bogdan					



### JTAG Connector



### USB-Blaster



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### block\_fpga

DATE	DESIGN	REV
D	2766 Rev. A	0
SCALE	SHEET	of
	4/7 -1	

H

H

G

G

F

F

E

E

D

D

C

C

B

B

A

A

ALTERA\_DATA0  
 GND  
 led\_0  
 USB\_FD1  
 TEMPDIODEBp  
 TEMPDIODEBn  
 USB\_FD11  
 USB\_FD15  
 nIO\_PULLUP  
 nCONFIG  
 Systemout  
 VCCIO8C  
 VCCIO6A  
 Systemout\_n  
 MSEL1  
 VCCIO7C  
 VCCIO1A  
 VCCBAT  
 USB\_PA2  
 USB\_FD1  
 led\_1  
 MSEL0  
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 VCC\_CLKIN7C  
 VREFB8CN0  
 USB\_SPARE  
 VCCPT  
 VCCA\_PLL\_T1  
 VCC\_CLKIN8C  
 USB\_PA5  
 USB\_PA3  
 USB\_FD4  
 VCCIO6C  
 USB\_FD0  
 VREFB6AN0  
 MSEL2  
 VCCD\_PLL\_T1  
 USB\_PA0  
 VREFB1AN0  
 USB\_WAKRUP  
 USB\_PA7  
 USB\_CTL2  
 USB\_FD2  
 USB\_FD5  
 VCCPD6A  
 VCCPD7C  
 VCCPD8C  
 USB\_PA1  
 USB\_IPCLK  
 USB\_CTL1  
 VCCIO1C  
 VCC  
 VCCL  
 VCCPD1A  
 USB\_PA4  
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 VCCPD1C  
 VCCPD1C  
 USB\_PA6  
 VREFB1CN0  
 GND+  
 VCCA\_PLL\_R2  
 VCCD\_PLL\_R2  
 VCCPD6C  
 USB\_CTL0  
 VCCD\_PLL\_L2  
 VCCA\_PLL\_L2  
 USB\_CLKOUT  
 USB\_FD6  
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 VCCPD5C  
 VCCPD2C  
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 VREFB2CN0  
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 Systemin0\_n  
 VREFB5CN0  
 USB\_FD7  
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 VCCPD4C  
 USB\_RDY1  
 VCCIO2C  
 VCCIO5A  
 VCCPD3C  
 VCCPD2A  
 VCCIO2A  
 USB\_RDY0  
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 Systemin1\_n  
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 VREFB2AN0  
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 USB\_FD9  
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 VCCA\_PLL\_B1  
 VCCD\_PLL\_B1  
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 nCE  
 PORSEL

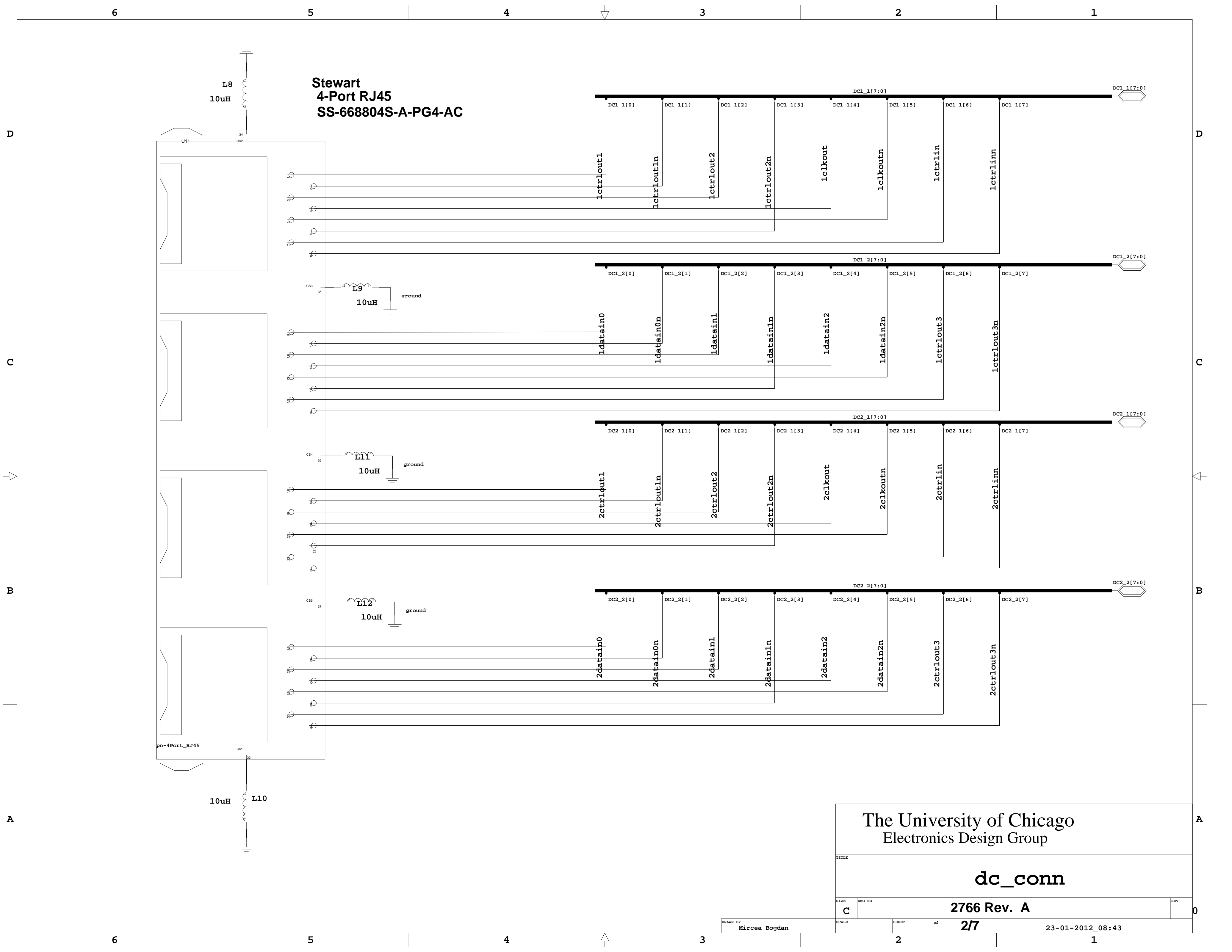
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 DC2in2  
 DC2in2\_n  
 DC1in2  
 DC1in2\_n  
 DC0out2  
 DC0out2\_n  
 ENET\_TX\_EN  
 ENET\_TX\_D2  
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 altera\_reserved\_tok  
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 DC0out1  
 altera\_reserved\_tdi  
 DC0out0\_n  
 DC0out0  
 DC1out2  
 DC1out1  
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 ENET\_TX\_D3  
 altera\_reserved\_ntrst  
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 DC1out1\_n  
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 DC2out0  
 ALTERA\_DATA4  
 debug19  
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 DC1out0  
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 ALTERA\_DATA1  
 ALTERA\_DATA1  
 ALTERA\_DATA7  
 ALTERA\_DATA6  
 ALTERA\_DATA6  
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 ALTERA\_DATA2  
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 debug18  
 debug17  
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 ENET\_led\_char\_err  
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 ENET\_RX  
 ENET\_RX\_n  
 ENET\_RX\_n  
 DC0in2\_n  
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 debug16  
 debug12  
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 ENET\_RX\_D7  
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 debug13  
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 DC1in1  
 DC0in0\_n  
 DC0in0  
 DC3in0\_n  
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 ENET\_RX\_D2  
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 DC3in3  
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 debug3  
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 ENET\_RESETRn  
 CONF\_DONE  
 CONF\_DONE  
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 DC3in3\_n  
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 DC3in1\_n  
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 DC2in3\_n  
 DC0in1\_n  
 DC0in1  
 ASDO  
 ASDO  
 ENET\_MDC  
 ENET\_MDC  
 DC2in3  
 DC2in3

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**block\_fpga**

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DRAWN BY	SCALE	SHEET OF
Mircea Bogdan		477-2

30-12-2011 11:06

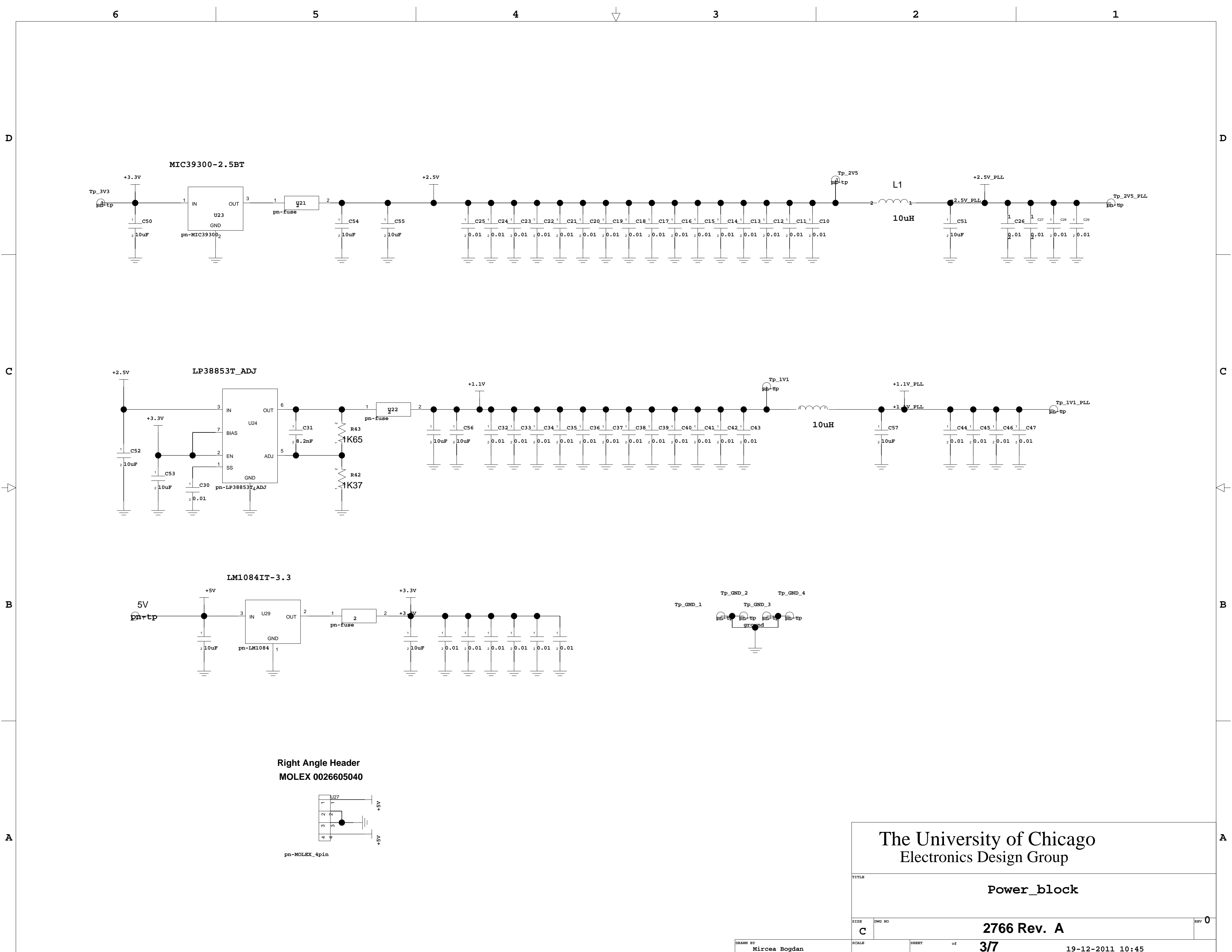


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TITLE

**dc\_conn**

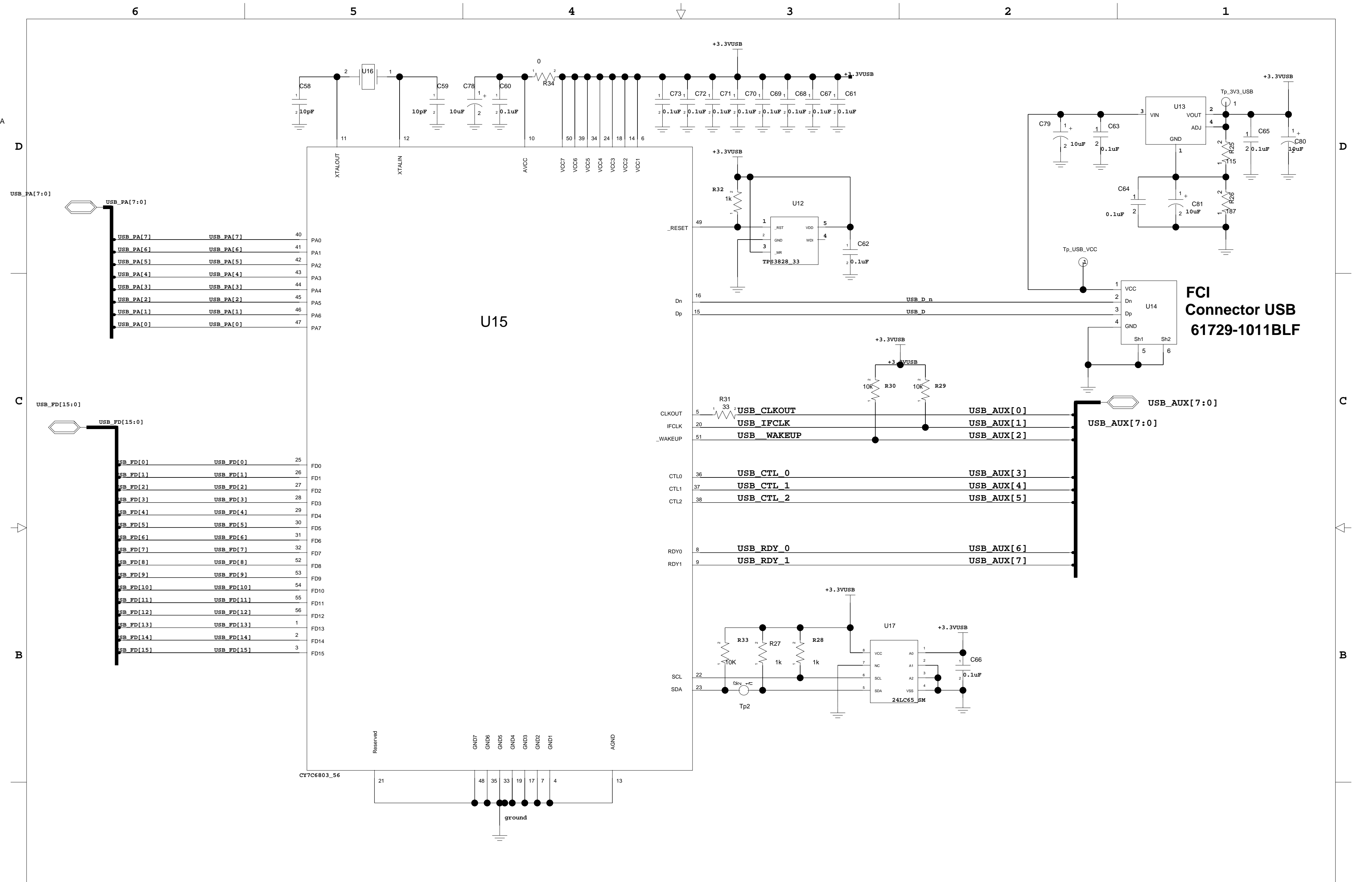
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DRAWN BY	SHEET	of	
Mircea Bogdan	<b>2/7</b>		
SCALE	23-01-2012_08:43		



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Power_block			
SIZE	DWG NO	2766 Rev. A	
C		of	3/7
SCALE	SHEET	of	19-12-2011_10:45

DRAWN BY  
Mircea Bogdan

REV 0



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TITLE

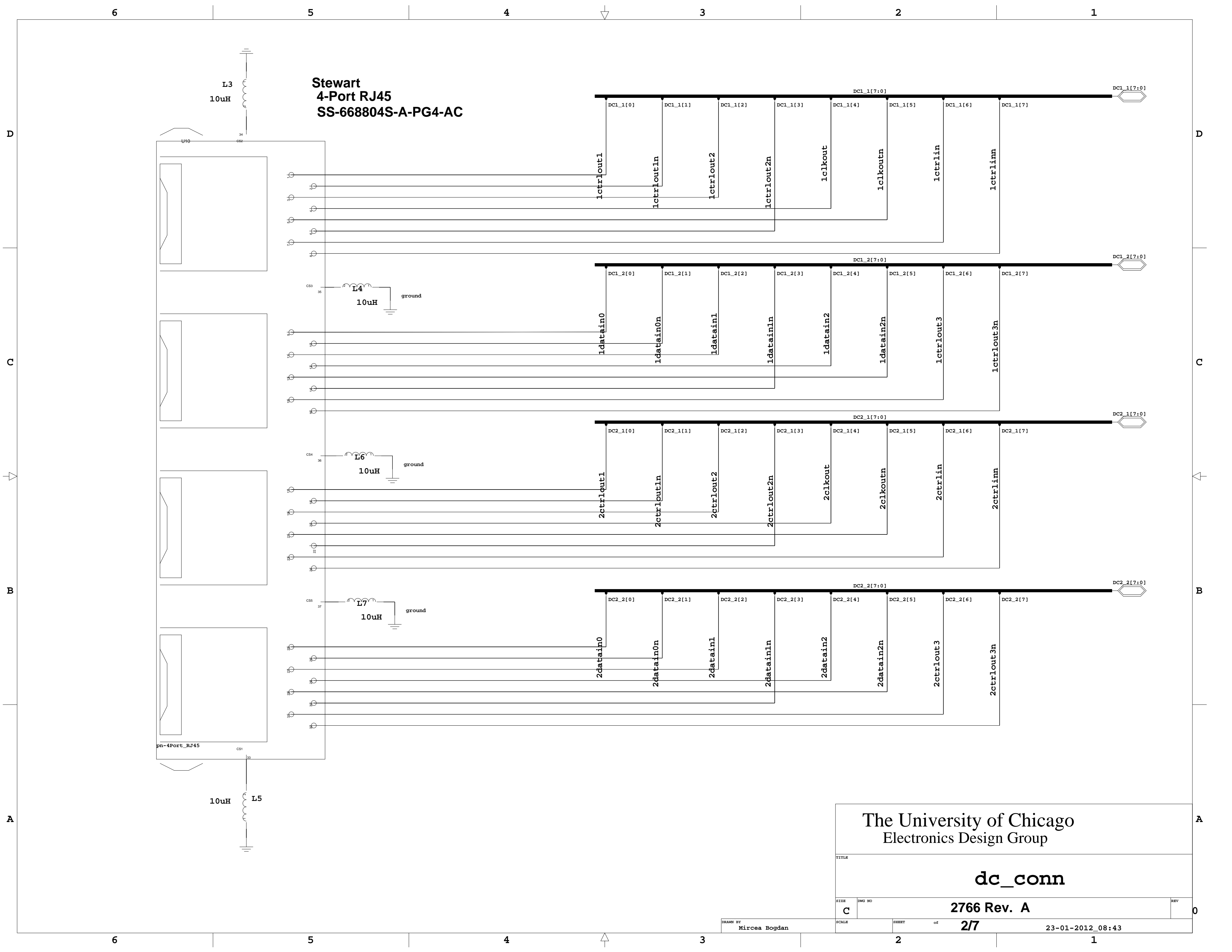
**usb**

SIZE C DWG NO 2766 Rev. A REV 0

SCALE SHEET 6/7 OF 6/7

09-01-2012\_15:47

DRAWN BY Mircea Bogdan



**Stewart  
4-Port RJ45  
SS-668804S-A-PG4-AC**

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TITLE

**dc\_conn**

SIZE	DWG NO	<b>2766 Rev. A</b>	REV
<b>C</b>			<b>0</b>
DRAWN BY	SHEET	of	
Mircea Bogdan	<b>2/7</b>		
SCALE	23-01-2012_08:43		

D

C

B

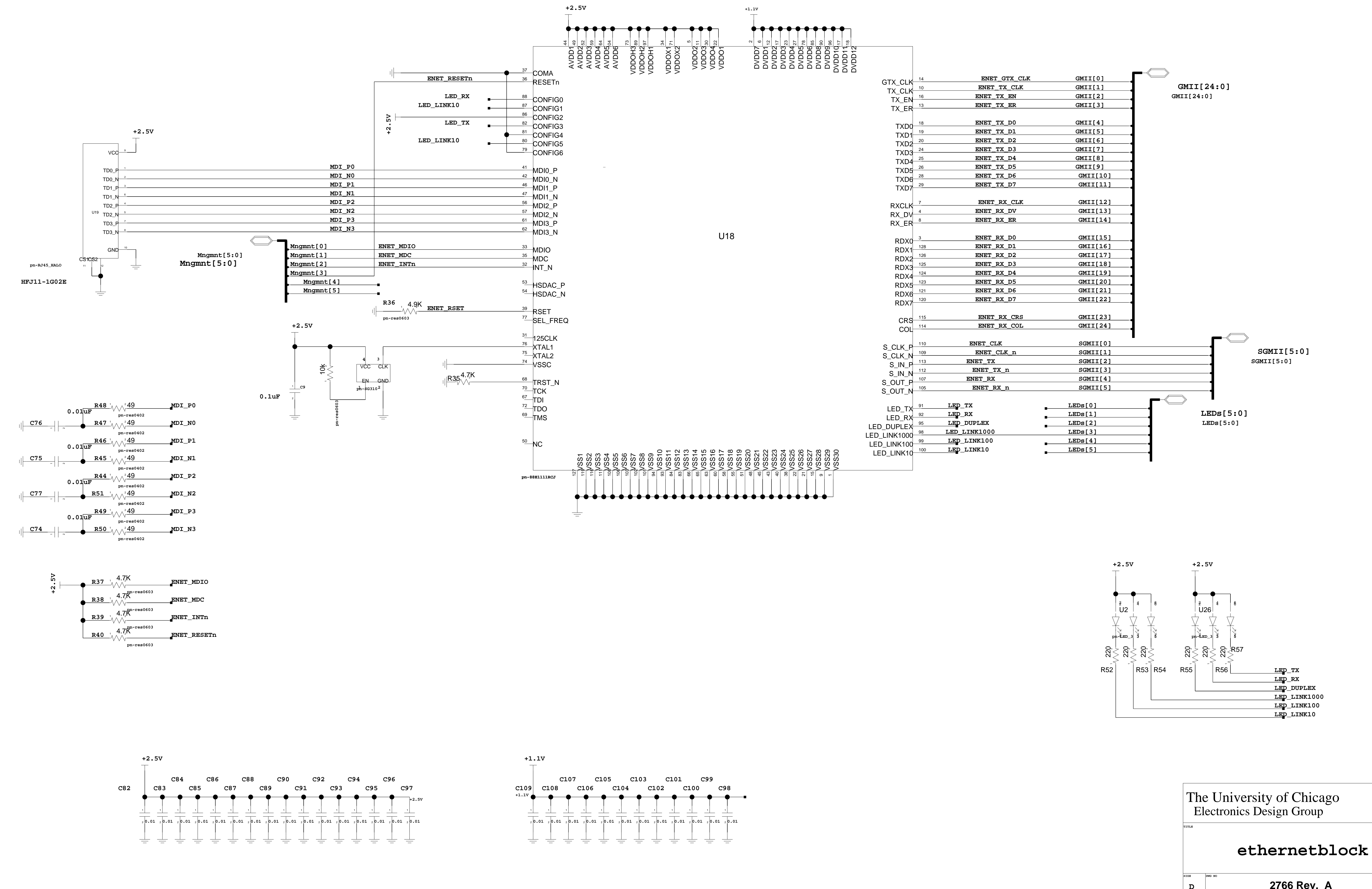
A

D

C

B

A



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**ethernetblock**

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DATE: D    DWG NO: 2766 Rev. A    REV: 0

SCALE: 7/7

DESIGNED BY: Mircea Bogdan

22-12-2011\_08:28



4

3

2

1

System[7:0]

System[7:0]

System[0]

System[1]

System[2]

System[3]

System[4]

System[5]

System[6]

System[7]

systemin0

systemin0\_n

systemin1

systemin1\_n

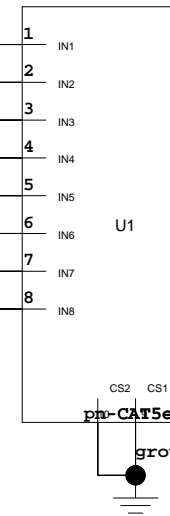
systemclk

systemclk\_n

systemout

systemout\_n

RJ45-Tyco 5406299-1



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TITLE

systemconn

SIZE

B

DWG NO

2766 Rev. A

REV

0

DRAWN BY

Mircea Bogdan

SCALE

SHEET

of

5/7

19-12-2011\_10:56

4

3

2



1

B



B

















A



A

 FPGA_Chip	 \$7831 ep3s50.1
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VREFB8CN0 / FPGA_Chip	VREFB8CN0 : ..	E13 : BI#
VREFB7CN0 / FPGA_Chip	VREFB7CN0 : ..	E10 : BI#
VREFB6CN0 / FPGA_Chip	VREFB6CN0 : ..	K5 : BI#
VREFB6AN0 / FPGA_Chip	VREFB6AN0 : ..	G5 : BI#
VREFB5CN0 / FPGA_Chip	VREFB5CN0 : ..	P5 : BI#
VREFB5AN0 / FPGA_Chip	VREFB5AN0 : ..	T5 : BI#
VREFB4CN0 / FPGA_Chip	VREFB4CN0 : ..	V10 : BI#
VREFB3CN0 / FPGA_Chip	VREFB3CN0 : ..	V12 : BI#
VREFB2CN0 / FPGA_Chip	VREFB2CN0 : ..	N18 : BI#
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VREFB1CN0 / FPGA_Chip	VREFB1CN0 : ..	K18 : BI#
VREFB1AN0 / FPGA_Chip	VREFB1AN0 : ..	G18 : BI#
VCC_CLKIN8C / FPGA_Chip	VCC_CLKIN8C	F13 : BI#
VCC_CLKIN7C / FPGA_Chip	VCC_CLKIN7C	E11 : BI#
VCC_CLKIN4C / FPGA_Chip	VCC_CLKIN4C	U10 : BI#
VCC_CLKIN3C / FPGA_Chip	VCC_CLKIN3C	T12 : BI#
VCCPT / FPGA_Chip	VCCPT : IN	...
VCCPGM / FPGA_Chip	VCCPGM : IN	...
VCCPD8C / FPGA_Chip	VCCPD8C : IN	H13 : BI#
VCCPD7C / FPGA_Chip	VCCPD7C : IN	H11 : BI#
VCCPD6C / FPGA_Chip	VCCPD6C : IN	L8 : BI#
VCCPD6A / FPGA_Chip	VCCPD6A : IN	H8 : BI#
VCCPD5C / FPGA_Chip	VCCPD5C : IN	N8 : BI#
VCCPD5A / FPGA_Chip	VCCPD5A : IN	P8 : BI#
VCCPD4C / FPGA_Chip	VCCPD4C : IN	P10 : BI#
VCCPD3C / FPGA_Chip	VCCPD3C : IN	R12 : BI#
VCCPD2C / FPGA_Chip	VCCPD2C : IN	N15 : BI#
VCCPD2A / FPGA_Chip	VCCPD2A : IN	R15 : BI#
VCCPD1C / FPGA_Chip	VCCPD1C : IN	K15 : BI#
VCCPD1A / FPGA_Chip	VCCPD1A : IN	J15 : BI#
VCCL / FPGA_Chip	VCCL : IN	...
VCCIO8C / FPGA_Chip	VCCIO8C : IN	...
VCCIO7C / FPGA_Chip	VCCIO7C : IN	E8 : BI# C8 : B...
VCCIO6C / FPGA_Chip	VCCIO6C : IN	G2 : BI# K5 : B...
VCCIO6A / FPGA_Chip	VCCIO6A : IN	D5 : BI# C3 : B...
VCCIO5C / FPGA_Chip	VCCIO5C : IN	R1 : BI# N7 : B...
VCCIO5A / FPGA_Chip	VCCIO5A : IN	R7 : BI# Y5 : B...
VCCIO4C / FPGA_Chip	VCCIO4C : IN	...
VCCIO3C / FPGA_Chip	VCCIO3C : IN	...
VCCIO2C / FPGA_Chip	VCCIO2C : IN	...
VCCIO2A / FPGA_Chip	VCCIO2A : IN	...
VCCIO1C / FPGA_Chip	VCCIO1C : IN	...
VCCIO1A / FPGA_Chip	VCCIO1A : IN	...
VCCD_PLL_T1 / FPGA_Chip	VCCD_PLL_T1	G12 : BI#
VCCD_PLL_R2 / FPGA_Chip	VCCD_PLL_R2	L6 : BI#
VCCD_PLL_L2 / FPGA_Chip	VCCD_PLL_L2	M17 : BI#




































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 VCCD_PLL_B1 / FPGA_Chip	VCCD_PLL_B1	U12 : BI#
 VCCBAT / FPGA_Chip	VCCBAT : IN	D4 : BI#
 VCCA_PLL_T1 / FPGA_Chip	VCCA_PLL_T1	F12 : BI#
 VCCA_PLL_R2 / FPGA_Chip	VCCA_PLL_R2	L5 : BI#
 VCCA_PLL_L2 / FPGA_Chip	VCCA_PLL_L2	M18 : BI#
 VCCA_PLL_B1 / FPGA_Chip	VCCA_PLL_B1	U11 : BI#
 VCC / FPGA_Chip	VCC : IN	...
 USB__WAKEUP / FPGA_Chip	USB__WAKEUP	G19 : BI#
 USB_SPARE / FPGA_Chip	USB_SPARE :	E22 : BI#
 USB_RDY1 / FPGA_Chip	USB_RDY1 : ...	P19 : BI#
 USB_RDY0 / FPGA_Chip	USB_RDY0 : ...	R18 : BI#
 USB_PA7 / FPGA_Chip	USB_PA7 : IN	G20 : BI#
 USB_PA6 / FPGA_Chip	USB_PA6 : IN	K16 : BI#
 USB_PA5 / FPGA_Chip	USB_PA5 : IN	F20 : BI#
 USB_PA4 / FPGA_Chip	USB_PA4 : IN	J19 : BI#
 USB_PA3 / FPGA_Chip	USB_PA3 : IN	F22 : BI#
 USB_PA2 / FPGA_Chip	USB_PA2 : IN	D22 : BI#
 USB_PA1 / FPGA_Chip	USB_PA1 : IN	H16 : BI#
 USB_PA0 / FPGA_Chip	USB_PA0 : IN	G15 : BI#
 USB_IFCLK / FPGA_Chip	USB_IFCLK : ...	H19 : BI#
 USB_FD9 / FPGA_Chip	USB_FD9 : IN	U8 : BI#
 USB_FD8 / FPGA_Chip	USB_FD8 : IN	V7 : BI#
 USB_FD7 / FPGA_Chip	USB_FD7 : IN	P6 : BI#
 USB_FD6 / FPGA_Chip	USB_FD6 : IN	N6 : BI#
 USB_FD5 / FPGA_Chip	USB_FD5 : IN	H2 : BI#
 USB_FD4 / FPGA_Chip	USB_FD4 : IN	G1 : BI#
 USB_FD3 / FPGA_Chip	USB_FD3 : IN	A4 : BI#
 USB_FD2 / FPGA_Chip	USB_FD2 : IN	H1 : BI#
 USB_FD15 / FPGA_Chip	USB_FD15 : ...	AB3 : BI#
 USB_FD14 / FPGA_Chip	USB_FD14 : ...	T4 : BI#
 USB_FD13 / FPGA_Chip	USB_FD13 : ...	U4 : BI#
 USB_FD12 / FPGA_Chip	USB_FD12 : ...	U7 : BI#
 USB_FD11 / FPGA_Chip	USB_FD11 : ...	AA1 : BI#
 USB_FD10 / FPGA_Chip	USB_FD10 : ...	V3 : BI#
 USB_FD1 / FPGA_Chip	USB_FD1 : IN	E2 : BI#
 USB_FD0 / FPGA_Chip	USB_FD0 : IN	G4 : BI#
 USB_CTL2 / FPGA_Chip	USB_CTL2 : ...	G22 : BI#
 USB_CTL1 / FPGA_Chip	USB_CTL1 : ...	H20 : BI#
 USB_CTL0 / FPGA_Chip	USB_CTL0 : ...	L16 : BI#
 USB_CLKOUT / FPGA_Chip	USB_CLKOUT	M19 : BI#
 TEMPDIODEp / FPGA_Chip	TEMPDIODEp :	A5 : BI#
 TEMPDIODEn / FPGA_Chip	TEMPDIODEn :	A6 : BI#
 Systemout_n / FPGA_Chip	Systemout_n :	C5 : BI#
 Systemout / FPGA_Chip	Systemout : ...	B5 : BI#
 Systemin1_n / FPGA_Chip	Systemin1_n :	R22 : BI#
 Systemin1 / FPGA_Chip	Systemin1 : IN	R21 : BI#


























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 Systemin0_n / FPGA_Chip	Systemin0_n :	N20 : Bl#
 Systemin0 / FPGA_Chip	Systemin0 : IN	N19 : Bl#
 PORSEL / FPGA_Chip	PORSEL : IN	Y18 : Bl#
 nSTATUS / FPGA_Chip	nSTATUS : IN	W18 : Bl#
 nIO_PULLUP / FPGA_Chip	nIO_PULLUP :	AB4 : Bl#
 nCSO / FPGA_Chip	nCSO : IN	Y6 : Bl#
 nCONFIG / FPGA_Chip	nCONFIG : IN	AB17 : B..
 nCEO / FPGA_Chip	nCEO : IN	U5 : Bl#
 nCE / FPGA_Chip	nCE : IN	Y17 : Bl#
 MSEL2 / FPGA_Chip	MSEL2 : IN	G7 : Bl#
 MSEL1 / FPGA_Chip	MSEL1 : IN	C6 : Bl#
 MSEL0 / FPGA_Chip	MSEL0 : IN	E7 : Bl#
 led_2 / FPGA_Chip	led_2 : IN	T7 : Bl#
 led_1 / FPGA_Chip	led_1 : IN	E3 : Bl#
 led_0 / FPGA_Chip	led_0 : IN	A2 : Bl#
 GND+ / FPGA_Chip	GND+ : IN	...
 GND / FPGA_Chip	GND : IN	...
 ENET_TX_n / FPGA_Chip	ENET_TX_n : ..	M16 : Bl#
 ENET_TX_ER / FPGA_Chip	ENET_TX_ER :	L20 : Bl#
 ENET_TX_EN / FPGA_Chip	ENET_TX_EN :	C12 : Bl#
 ENET_TX_D7 / FPGA_Chip	ENET_TX_D7 :	L19 : Bl#
 ENET_TX_D6 / FPGA_Chip	ENET_TX_D6 :	K21 : Bl#
 ENET_TX_D5 / FPGA_Chip	ENET_TX_D5 :	AB14 : B..
 ENET_TX_D4 / FPGA_Chip	ENET_TX_D4 :	J22 : Bl#
 ENET_TX_D3 / FPGA_Chip	ENET_TX_D3 :	F15 : Bl#
 ENET_TX_D2 / FPGA_Chip	ENET_TX_D2 :	D12 : Bl#
 ENET_TX_D1 / FPGA_Chip	ENET_TX_D1 :	F14 : Bl#
 ENET_TX_D0 / FPGA_Chip	ENET_TX_D0 :	A12 : Bl#
 ENET_TX_CLK / FPGA_Chip	ENET_TX_CLK	G21 : Bl#
 ENET_TX / FPGA_Chip	ENET_TX : BI	M15 : Bl#
 ENET_RX_n / FPGA_Chip	ENET_RX_n : ..	N22 : Bl#
 ENET_RX_ER / FPGA_Chip	ENET_RX_ER :	R20 : Bl#
 ENET_RX_DV / FPGA_Chip	ENET_RX_DV :	T17 : Bl#
 ENET_RX_D7 / FPGA_Chip	ENET_RX_D7 :	P16 : Bl#
 ENET_RX_D6 / FPGA_Chip	ENET_RX_D6 :	P17 : Bl#
 ENET_RX_D5 / FPGA_Chip	ENET_RX_D5 :	R19 : Bl#
 ENET_RX_D4 / FPGA_Chip	ENET_RX_D4 :	T19 : Bl#
 ENET_RX_D3 / FPGA_Chip	ENET_RX_D3 :	T15 : Bl#
 ENET_RX_D2 / FPGA_Chip	ENET_RX_D2 :	U19 : Bl#
 ENET_RX_D1 / FPGA_Chip	ENET_RX_D1 :	U16 : Bl#
 ENET_RX_D0 / FPGA_Chip	ENET_RX_D0 :	U15 : Bl#
 ENET_RX_CRS / FPGA_Chip	ENET_RX_CRS	R13 : Bl#
 ENET_RX_COL / FPGA_Chip	ENET_RX_COL	W12 : Bl#
 ENET_RX_CLK / FPGA_Chip	ENET_RX_CLK	W14 : Bl#
 ENET_RX / FPGA_Chip	ENET_RX : BI	N21 : Bl#
ENET_RESETn / FPGA_Chip	ENET_RESETn	V13 : Bl#

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 ENET_MDIO / FPGA_Chip	ENET_MDIO : ..	U13 : BI#
 ENET_MDC / FPGA_Chip	ENET_MDC : ...	Y12 : BI#
 ENET_LED_LINK1000 / FPGA_Chip	ENET_LED_LIN	W13 : BI#
 ENET_led_disp_err / FPGA_Chip	ENET_led_disp	AA15 : B..
 ENET_led_char_err / FPGA_Chip	ENET_led_char	N17 : BI#
 ENET_led_an / FPGA_Chip	ENET_led_an :	P20 : BI#
 ENET_INTn / FPGA_Chip	ENET_INTn : ...	U14 : BI#
 ENET_GTX_CLK / FPGA_Chip	ENET_GTX_CL	T13 : BI#
 ENET_CLK_n / FPGA_Chip	ENET_CLK_n :	M22 : BI#
 ENET_CLK / FPGA_Chip	ENET_CLK : ...	M21 : BI#
 ENETled_link / FPGA_Chip	ENETled_link :	N16 : BI#
 DNU / FPGA_Chip	DNU : BI	L12 : BI#
 debug9 / FPGA_Chip	debug9 : BI	K4 : BI#
 debug8 / FPGA_Chip	debug8 : BI	H3 : BI#
 debug7 / FPGA_Chip	debug7 : BI	M6 : BI#
 debug6 / FPGA_Chip	debug6 : BI	N2 : BI#
 debug5 / FPGA_Chip	debug5 : BI	M7 : BI#
 debug4 / FPGA_Chip	debug4 : BI	F21 : BI#
 debug3 / FPGA_Chip	debug3 : BI	V6 : BI#
 debug2 / FPGA_Chip	debug2 : BI	AB1 : BI#
 debug19 / FPGA_Chip	debug19 : BI	J1 : BI#
 debug18 / FPGA_Chip	debug18 : BI	N4 : BI#
 debug17 / FPGA_Chip	debug17 : BI	N5 : BI#
 debug16 / FPGA_Chip	debug16 : BI	P4 : BI#
 debug15 / FPGA_Chip	debug15 : BI	P3 : BI#
 debug14 / FPGA_Chip	debug14 : BI	V4 : BI#
 debug13 / FPGA_Chip	debug13 : BI	R6 : BI#
 debug12 / FPGA_Chip	debug12 : BI	P7 : BI#
 debug11 / FPGA_Chip	debug11 : BI	T8 : BI#
 debug10 / FPGA_Chip	debug10 : BI	N3 : BI#
 DCrefclock_n / FPGA_Chip	DCrefclock_n :	K1 : BI#
 DCrefclock / FPGA_Chip	DCrefclock : ...	K2 : BI#
 DCLK / FPGA_Chip	DCLK : BI	Y4 : BI#
 DC3out2_n / FPGA_Chip	DC3out2_n : ...	K7 : BI#
 DC3out2 / FPGA_Chip	DC3out2 : BI	K8 : BI#
 DC3out1_n / FPGA_Chip	DC3out1_n : ...	L3 : BI#
 DC3out1 / FPGA_Chip	DC3out1 : BI	L4 : BI#
 DC3out0_n / FPGA_Chip	DC3out0_n : ...	M3 : BI#
 DC3out0 / FPGA_Chip	DC3out0 : BI	M4 : BI#
 DC3in3_n / FPGA_Chip	DC3in3_n : BI	W1 : BI#
 DC3in3 / FPGA_Chip	DC3in3 : BI	V1 : BI#
 DC3in2_n / FPGA_Chip	DC3in2_n : BI	T1 : BI#
 DC3in2 / FPGA_Chip	DC3in2 : BI	T2 : BI#
 DC3in1_n / FPGA_Chip	DC3in1_n : BI	W2 : BI#
 DC3in1 / FPGA_Chip	DC3in1 : BI	W3 : BI#
 DC3in0_n / FPGA_Chip	DC3in0_n : BI	U3 : BI#

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 DC3in0 / FPGA_Chip	DC3in0 : BI	T3 : BI#
 DC2out2_n / FPGA_Chip	DC2out2_n : ...	H4 : BI#
 DC2out2 / FPGA_Chip	DC2out2 : BI	H5 : BI#
 DC2out1_n / FPGA_Chip	DC2out1_n : ...	J3 : BI#
 DC2out1 / FPGA_Chip	DC2out1 : BI	J4 : BI#
 DC2out0_n / FPGA_Chip	DC2out0_n : ...	J7 : BI#
 DC2out0 / FPGA_Chip	DC2out0 : BI	H7 : BI#
 DC2in3_n / FPGA_Chip	DC2in3_n : BI	W22 : BI#
 DC2in3 / FPGA_Chip	DC2in3 : BI	Y22 : BI#
 DC2in2_n / FPGA_Chip	DC2in2_n : BI	AB19 : B..
 DC2in2 / FPGA_Chip	DC2in2 : BI	AB18 : B..
 DC2in1_n / FPGA_Chip	DC2in1_n : BI	T21 : BI#
 DC2in1 / FPGA_Chip	DC2in1 : BI	T20 : BI#
 DC2in0_n / FPGA_Chip	DC2in0_n : BI	AA22 : B..
 DC2in0 / FPGA_Chip	DC2in0 : BI	AA21 : B..
 DC1out2_n / FPGA_Chip	DC1out2_n : ...	G6 : BI#
 DC1out2 / FPGA_Chip	DC1out2 : BI	F7 : BI#
 DC1out1_n / FPGA_Chip	DC1out1_n : ...	G8 : BI#
 DC1out1 / FPGA_Chip	DC1out1 : BI	F8 : BI#
 DC1out0_n / FPGA_Chip	DC1out0_n : ...	J6 : BI#
 DC1out0 / FPGA_Chip	DC1out0 : BI	H6 : BI#
 DC1in3_n / FPGA_Chip	DC1in3_n : BI	V22 : BI#
 DC1in3 / FPGA_Chip	DC1in3 : BI	V21 : BI#
 DC1in2_n / FPGA_Chip	DC1in2_n : BI	AB21 : B..
 DC1in2 / FPGA_Chip	DC1in2 : BI	AB20 : B..
 DC1in1_n / FPGA_Chip	DC1in1_n : BI	T22 : BI#
 DC1in1 / FPGA_Chip	DC1in1 : BI	U22 : BI#
 DC1in0_n / FPGA_Chip	DC1in0_n : BI	W21 : BI#
 DC1in0 / FPGA_Chip	DC1in0 : BI	W20 : BI#
 DC0out2_n / FPGA_Chip	DC0out2_n : ...	C4 : BI#
 DC0out2 / FPGA_Chip	DC0out2 : BI	B4 : BI#
 DC0out1_n / FPGA_Chip	DC0out1_n : ...	E4 : BI#
 DC0out1 / FPGA_Chip	DC0out1 : BI	E5 : BI#
 DC0out0_n / FPGA_Chip	DC0out0_n : ...	F3 : BI#
 DC0out0 / FPGA_Chip	DC0out0 : BI	F4 : BI#
 DC0in3_n / FPGA_Chip	DC0in3_n : BI	R3 : BI#
 DC0in3 / FPGA_Chip	DC0in3 : BI	R4 : BI#
 DC0in2_n / FPGA_Chip	DC0in2_n : BI	P1 : BI#
 DC0in2 / FPGA_Chip	DC0in2 : BI	P2 : BI#
 DC0in1_n / FPGA_Chip	DC0in1_n : BI	Y1 : BI#
 DC0in1 / FPGA_Chip	DC0in1 : BI	Y2 : BI#
 DC0in0_n / FPGA_Chip	DC0in0_n : BI	U1 : BI#
 DC0in0 / FPGA_Chip	DC0in0 : BI	U2 : BI#
 CONF_DONE / FPGA_Chip	CONF_DONE :	V18 : BI#
 CLOCKIN_n / FPGA_Chip	CLOCKIN_n : ..	AB13 : B..
 CLOCKIN / FPGA_Chip	CLOCKIN : BI	AA13 : B..

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 ASDO / FPGA_Chip	ASDO : BI	Y3 : BI#
 altera_reserved_tms / FPGA_Chip	altera_reserved	D17 : BI#
 altera_reserved_tdo / FPGA_Chip	altera_reserved	A18 : BI#
 altera_reserved_tdi / FPGA_Chip	altera_reserved	E17 : BI#
 altera_reserved_tck / FPGA_Chip	altera_reserved	D18 : BI#
 altera_reserved_ntrst / FPGA_Chip	altera_reserved	F18 : BI#
 ALTERA_DATA7 / FPGA_Chip	ALTERA_DATA	J20 : BI#
 ALTERA_DATA6 / FPGA_Chip	ALTERA_DATA	J21 : BI#
 ALTERA_DATA5 / FPGA_Chip	ALTERA_DATA	J16 : BI#
 ALTERA_DATA4 / FPGA_Chip	ALTERA_DATA	H17 : BI#
 ALTERA_DATA3T / FPGA_Chip	ALTERA_DATA	K19 : BI#
 ALTERA_DATA2 / FPGA_Chip	ALTERA_DATA	K20 : BI#
 ALTERA_DATA1 / FPGA_Chip	ALTERA_DATA	J17 : BI#
 ALTERA_DATA0 / FPGA_Chip	ALTERA_DATA	J18 : BI#