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C

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A

D

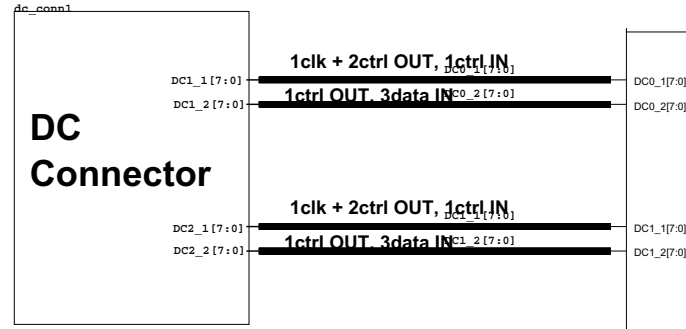
C

B

A

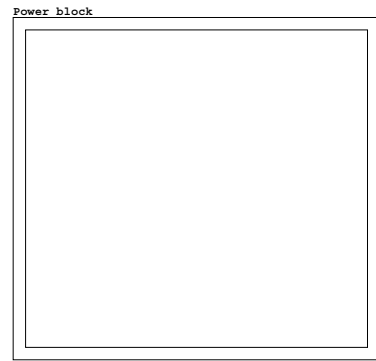
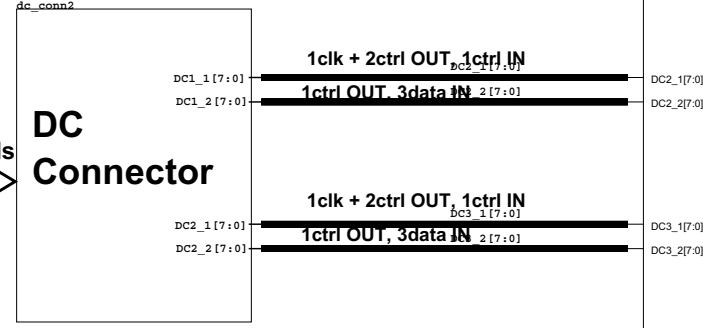
To/From Digital Cards  
Left Side →

**DC Connector**



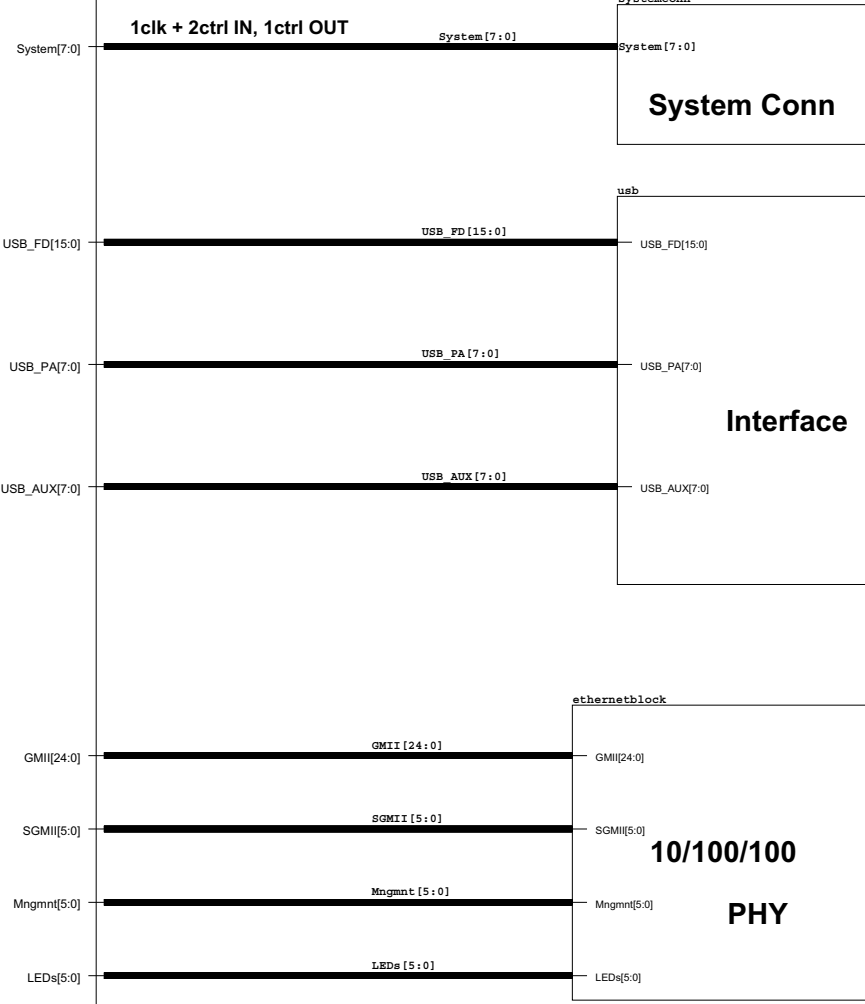
To/From Digital Cards  
Right Side →

**DC Connector**



**Block\_FPGA**

Sheet\_2\_4



The University of Chicago  
Electronics Design Group

TITLE			
<b>psec_cc Top Level</b>			
SIZE	DWG NO	REV	
C		2766 Rev. A	0
SCALE	SHEET	of	DATE
	1/7		06-01-2012 12:08

DRAWN BY  
Mircea Bogdan

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