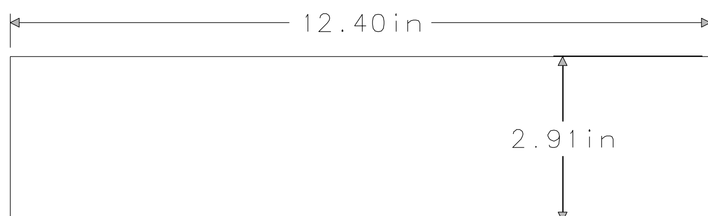
B2597 BOARD SIZE (315mmx74mm)



BOARD's DRILL SCHEDULE (Inch)

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Min/Max
○	.01	876	YES	---
⊞	.016	355	YES	---
Φ	.02	50	YES	---
⊟	.035	320	YES	---
⊖	.041	38	YES	---
◫	.055	4	YES	---
⊕	.1063	13	YES	---

BOARD SPECIFICATIONS

1. Board Layers: 12
2. Layer Stack Order:

Layer	Description
Layer1 (Artwork_1):	Top component layer (Signal_1), 0.5oz
Layer2 (Artwork_2):	Power_1 (VCC), 1oz
Layer3 (Artwork_3):	Power_2 (GROUND), 0.5oz
Layer4 (Artwork_4):	Inner: Signal_3 0.5oz
Layer5 (Artwork_5):	Inner Signal_4, 0.5oz
Layer6 (Artwork_6):	Power_2 (GROUND), 0.5oz
Layer7 (Artwork_7):	Power_2 (GROUND), 0.5oz
Layer8 (Artwork_8):	Inner Signal_5, 0.5oz
Layer9 (Artwork_9):	Inner Signal_6, 0.5oz
Layer10 (Artwork_10):	Power_2 (GROUND), 0.5oz
Layer11(Artwork_11):	Power_3 (VINIT), 1oz
Layer12(Artwork_12):	Bottom component layer (signal_2), 0.5oz

3. Apply silkscreen on both side:
   Artwork_13: Top silkscreen.
   Artwork_14: Bottom silkscreen
4. Apply solder mask over bare copper on both side:
   Artwork_15: Top solder mask
   Artwork_16: Bottom solde mask
5. Material: FR406 (Tc>150c)
6. Board thickness: 0.072'' +/- 0.010.
7. Trace impedance for all the signal layers: 50 ohms +/- 10%.
8. Copper thickness 1oz before plating for all the power planes.
9. Copper thickness 0.5oz before plating for all the signal layers.
10. Ni/Au plating (3 to 8 micro-inches soft gold) over bare copper
11. All layers mininum trace width/clearence 0.005"/0.005"
12. All dimensions are in inches unless otherwise noted.

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SCHM# B2596
SPEC# B2597
ASSM# B2598

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
B2579 Specification

SHEET 1 OF 1
DATE 11/30/2006
DRAWN TANG

B- 2597
REV 1.0