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Conceptual Design of a Deadtimeless Trigger for the CDF Trigger Upgrade

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Abstract

As has been described elsewhere [1, 2, 3] the front-end and trigger must be upgraded to accommodate the shorter bunch spacing ($132 - 396$ ns) and higher luminosity ($\approx 10^{32}$) planned for RUN II and beyond. This note describes an upgrade design using an all digital deadtimeless trigger. The advantage of a deadtimeless trigger system is that the rate out of each level approaches the average rate at which the next level can process. For example, with a second level processing time of 20 μs a level 1 rate of 5 kHz will yield 10% deadtime. However, if the system is buffered at level 2 (i.e. deadtimeless) a level 1 rate of almost 50 kHz can be achieved with nearly zero deadtime[4].

1 General Overview

The basic design of the CDF trigger upgrade consists of 2 hardware levels both of which are buffered. Figure 1 shows the dataflow and buffering for the DAQ and trigger paths in the upgrade. Data to be used in the Level 1 (L1) trigger is digitized every beam crossing and sent to the L1 portion of the trigger. While the Level 1 trigger decision is being made, all data from the detector is stored in L1 buffers for readout and/or use at Level 2 (L2). On a L1 accept the data from the L1 buffer is passed to a L2 buffer and the event is queued for a L2 decision. On a L2 accept the L2 buffer for that event is queued for readout into the L3 processor farm. After readout or on a L2 reject the L2 buffer is freed for use by a later L1 accept.

The Level 1 trigger is a synchronous system with an event read in every beam crossing and a decision (L1 accept/L1 reject) made every beam crossing. The depth of the L1 decision pipeline is expected to be approximately $4\mu s$ (L1 Latency). The L1 buffers must be at least as deep as this processing pipeline or the data associated with a particular L1 decision would be lost before the decision is made. At a bunch spacing of $132\mu s$, a buffer 32 events deep provides storage for 4224 ns. The L1 buffer is 42 crossings deep (5544 ns) to provide a margin for unanticipated increases in the L1 latency. The equivalent depth with a 396 ns bunch spacing is 14 crossings.

The Level 2 trigger is an asynchronous system which processes events that have received a L1 accept in a time ordered fashion. It is structured as a two stage pipeline with data buffering at the input of each stage. The first stage is based on dedicated hardware processors which assemble information from a particular section of the detector (Calorimeter Clusters, SVX tracks etc). The second stage consists of programmable processors (DEC Alpha processors) operating on lists of objects generated by the first stage. Each of the L2 stages is expected to take approximately $10\mu s$ giving a latency of approximately $20\mu s$.

Storage of four events is provided in the L2 buffers. A simulation of the trigger and DAQ upgrade[4] has shown that for a L2 execution time of 20μsec, a DAQ readout time of 500μsec and accept rates of 40kHz at L1 and 1kHz at L2 the deadtime would be approximately 10%. By comparison if the L2 buffer is only 1 event 10% deadtime is reached at a L1 accept rate of less than 5kHz. Since this simulation modeled a L2 system with only one stage, it should provide conservative estimates for the system with 2 stages each taking 10μsec.

2 Trigger Data Flow

Trigger decisions are based on information from calorimeter towers (CAL), central strip chambers (CES), central tracking chamber (CTC), muon chambers and muon scintilators and silicon vertex detector. The data flow from the detector elements through Level 1 and Level 2 is shown in Figure 2. Each small box in the figure indicates a trigger subsystem which generates inputs to the Global L1 or Global L2 decision modules.

The Trigger Supervisor Interface (TSI) provides an interface between the trigger system and the DAQ and Clock. The TSI also manages the four L2 buffers used for DAQ readout on frontend and trigger boards. The TSI distributes global trigger signals to the rest of the trigger and DAQ. Among the signals distributed by the TSI distributes are L1A/R, L2A/R, a global clock and the bunch crossing signal.

2.1 Level 1 Data Flow

The Level 1 trigger decision will be made on transverse energy in the calorimeter, tracks in the CTC and track stubs found in the CMU, CMP and CMX muon chambers. Figure 3 shows a block diagram of the Level 1 trigger. There are four basic stages to the Level 1 system:

1. Generate Muon primitives (stubs) on TDC AUX cards. CTC track primitives are generated by the eXtremely Fast Tracker (XFT) [5]. Calorimeter energies for trigger towers are summed on front-end cards.
2. Track primitives from the XFT are prepared for other subsystems and fanned out by the track extrapolation unit (XTRP).
3. Trigger objects (e's, μ's, jets, hadronic B's etc.) are formed using combinations of primitives and cuts on those primitives. Calorimeter based objects (e's, jets, photons) are formed in L1CAL, Muon's are formed in MU2P and hadronic B's are formed in L1TRACK.
4. The number of each type of trigger object is fed to L1 GLOBAL (FRED) which forms L1 accept/reject based on these objects.

The L1CAL subsystem[6] uses transverse energy summed into *Trigger Towers* of approximately $0.2 \times 15°$ in $\eta - \phi$ space[7] and tracks from the XFT track processor to form electron, photon and jet trigger objects. Eight different triggers are allowed for the electromagnetic calorimeter and another eight for the hadronic calorimeters which are processed independently. Each trigger can consist of an energy threshold (may be η dependent) and a track p_t threshold. The number of trigger towers which pass each of the 16 triggers is passed to GLOBAL L1 for trigger decision. L1CAL also calculates the ΣE_T and missing E_T for the event for use by L1 GLOBAL.

The MU2P subsystem uses muon primitives and XFT tracks extrapolated to the muon chambers by the XTRP to form muon trigger objects. Coincidence with muon scintillators where applicable is used to remove muon stubs from other crossings. Different muon objects can be formed based on chamber systems traversed and track p_t. The number of each muon object type found is passed to L1 Global.

The L1 Track subsystem is designed to trigger purely on tracks in the CTC to provide an efficient trigger path for hadronic B decays. A list of tracks with p_t greater than some threshold ($\sim$ 2.0 GeV/c) is fed to L1TRACK by the XTRP. Trigger objects are formed using combinations of p_t and ϕ of these tracks. The presence or absence of each of these trigger objects is passed to L1 Global decision.

L1GLOBAL (FRED) makes the L1 trigger decision based on the quantity of each trigger object passed to it. This decision is then passed to the TSI for distribution to the rest of the trigger and DAQ.

2.2 Level 2 Data Flow

The Level 2 system is separated into a two step pipeline. The first stage of the pipeline consists of two parts: generating primitives in dedicated hardware and reading primitives generated by L1 and L2 hardware into memory. The second pipeline stage is carried out using L2 Alpha processors based on the DEC Alpha chip. The primitives loaded into memory in the first stage of L2 are available for use by the L2 processors.

The Level 2 trigger has available as inputs the trigger primitives generated for L1: Trigger Tower energies, XFT tracks and muon stubs. Additional data for Level 2 come from the shower maximum strip chambers in the central calorimeter and the $r - \phi$ strips of SVX II. There are three hardware subsystems generating primitives at Level 2: L2CAL, XCES and Silicon Vertex Tracker (SVT).

The L2CAL hardware carries out the hardware cluster finder functions. It receives trigger tower energies from the L1 CAL hardware (DRAW boards) and applies seed and shoulder thresholds for clusterfinding.

The XCES system consists of threshold cut(s) applied on the front end cards and track matching hardware at L2. The output of the threshold application is a bitmap of strips above threshold with a segmentation of 8 bits per 15° wedge. The tracks found by the XFT are extrapolated by the XTRP to the showermax radius and fed to XCES where they are matched with the strip bitmap.

The SVT uses hits from the $r - \phi$ strips of SVX II and tracks from the XFT to find tracks in SVX II. The SVT improves on the XFT resolution for ϕ_0 and p_t and adds a measurement of the track impact parameter (d).

After the L2CAL, XCES and SVT have finished processing data for a given event, the output of these devices is fed to memory in the L2 processor crate. There are two separate memories, while one is being used by the Alpha processors another is available for loading with data for the next event to be processed.

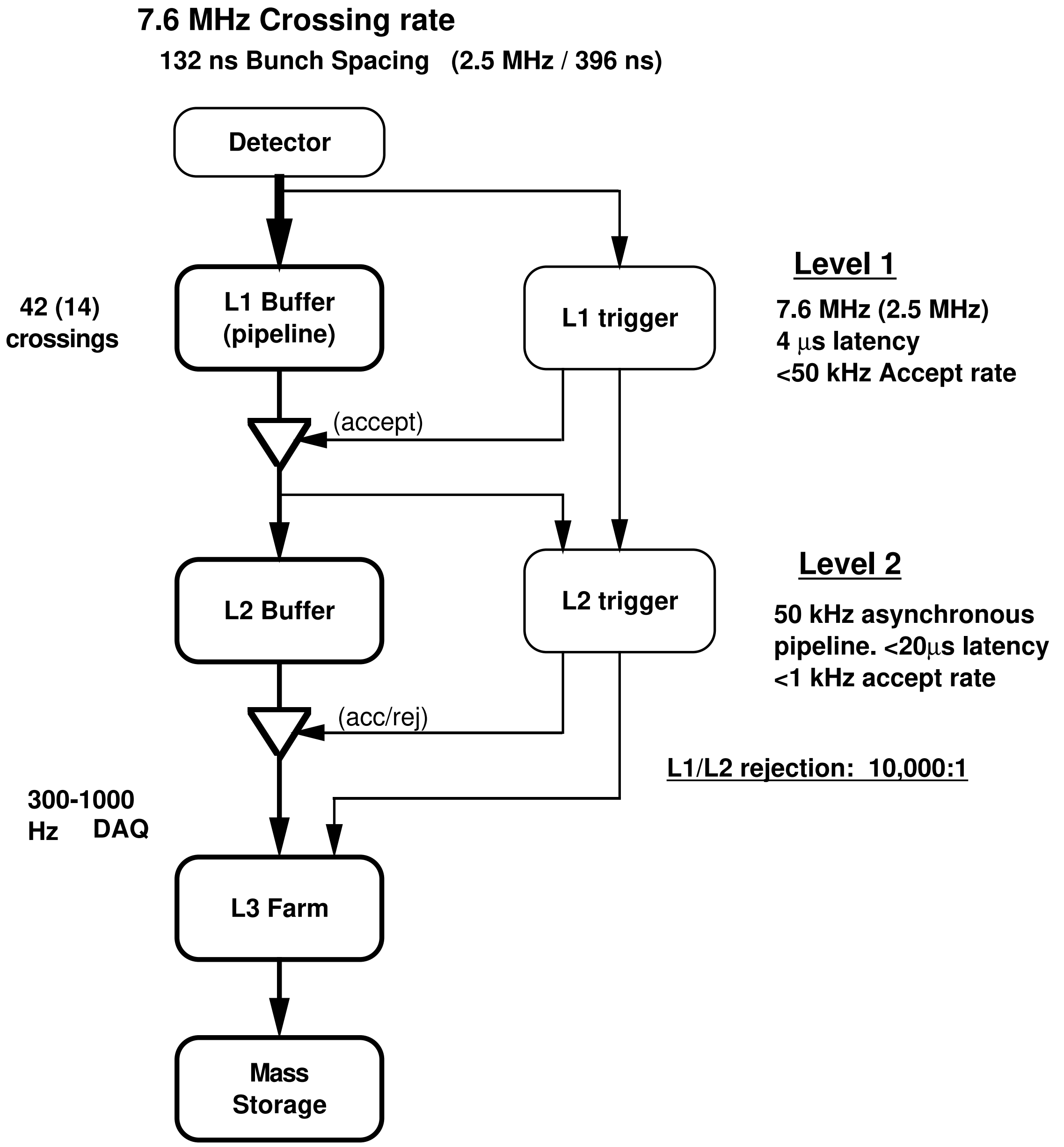

Figure 1: Dataflow for the CDF detector deadtimeless trigger/DAQ upgrade. The upgrade is designed to accommodate bunch crossings of 132 ns, or multiples of 132 ns. The front-ends buffer the data in $4\mu s$ pipelines while the level 1 trigger processes the data and makes a trigger decision. For each level 1 accept the data is stored in a L2/DAQ buffer while the Level 2 trigger works. A level 2 accept initiates the readout of the event data into the Level 3 processor farm where an accept causes the data to be written to disk/tape.

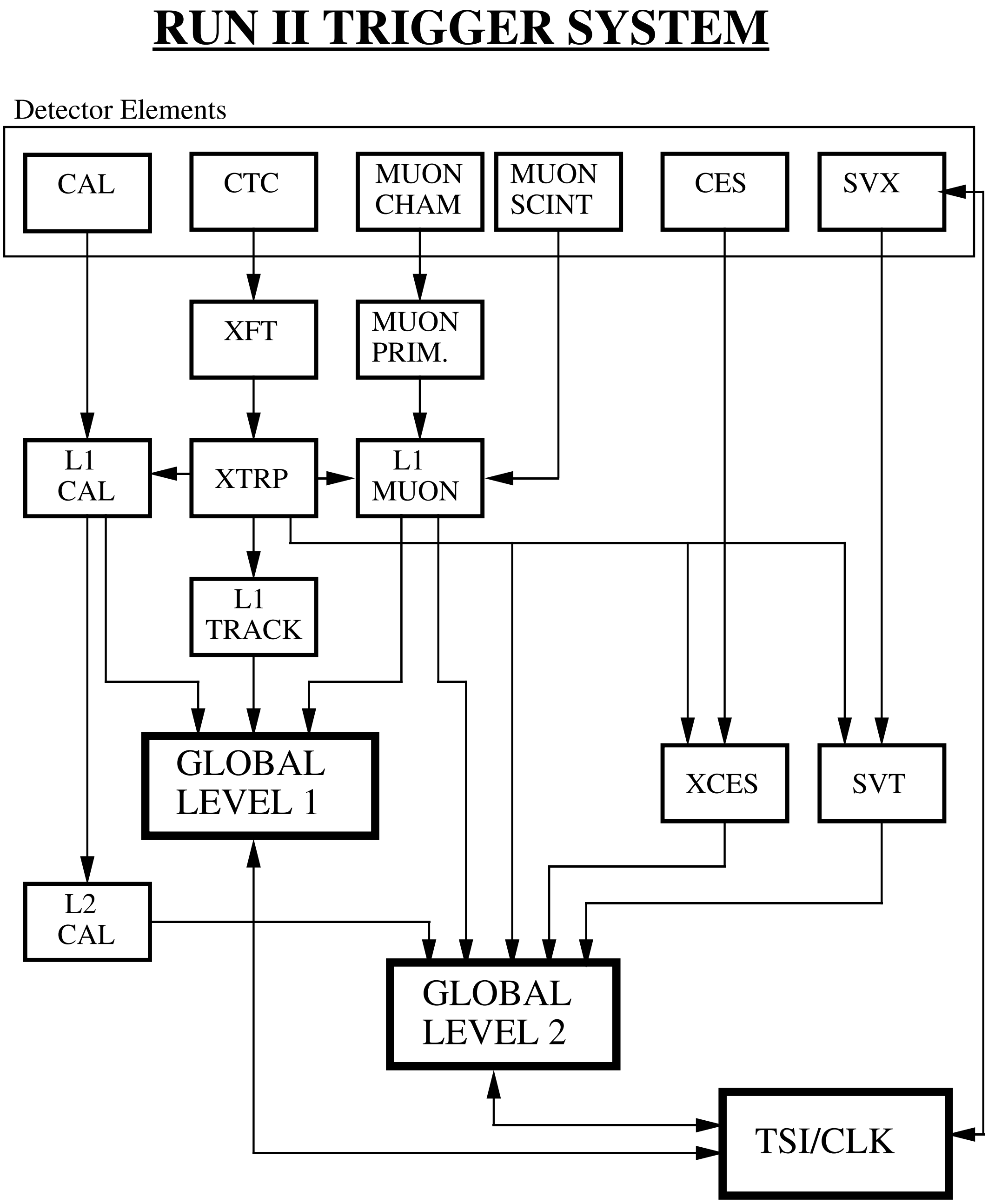

Figure 2: Block diagram of the CDF trigger upgrade. Small blocks represent trigger hardware subsystems which feed the L1 and L2 Global decision blocks. TSI/CLK provides clock and beam crossing signals. In addition the TSI distributes global trigger signals such as L1 accept, L2 accept/reject and L2 buffer number to the rest of the trigger and DAQ.

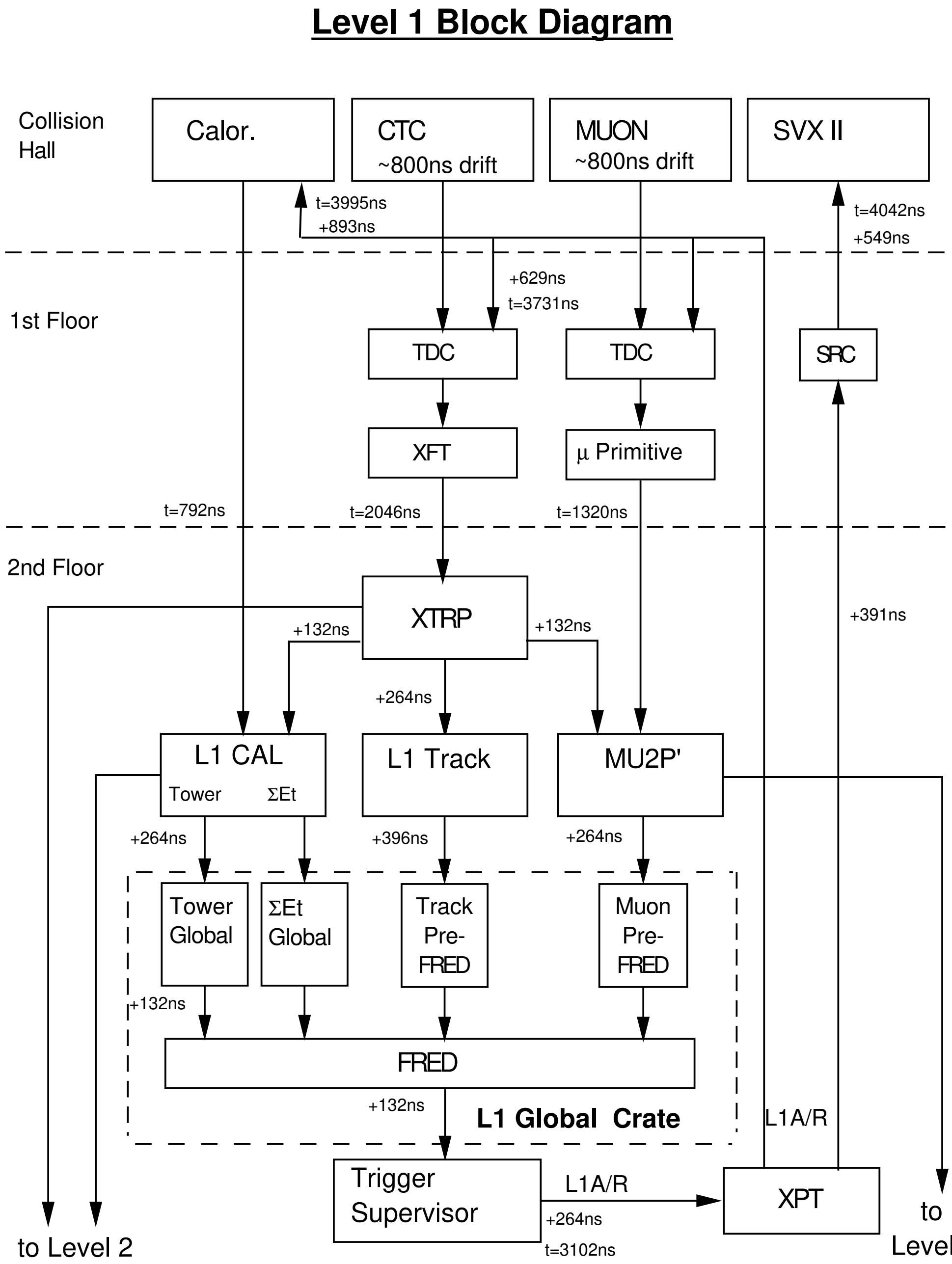

Figure 3: Block diagram and data flow for Level 1 in the CDF trigger upgrade. Detector elements are: calorimeter towers (CAL), central strip chambers (CES), muon chambers, muon scintillators and silicon vertex detector. Trigger towers are summed on front-end cards. Times indicated by $t =$ are approximate elapsed time from beam crossing while times indicated by $+$ are approximate execution time of previous block. The crosspoint (XPT) and SVX detector are included to illustrate timing of Level 1 system.

References

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[4] H. Kasha and M.P. Schmidt, *Simulations of the Run II Trigger/DAQ Upgrade*, CDF/DOC/TRIGGER/CDFR/2306, 1994.

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[6] H. Frisch, M. Shochet, G. Sullivan, D. Toback, J. Wahl and P. Wilson *Conceptual Design of the L1 Calorimeter Trigger for the Run II Upgrade*, CDF/DOC/TRIGGER/CDFR/2909, 1994.

[7] H. Frisch, M. SHochet, G. Sullivan and P.J. Wilson, *Trigger Tower organization and summing in $\eta - \phi$ space for Run II and beyond*, CDF/DOC/TRIGGER/CDFR/2045, 1994.