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Specification of DAQ/Trigger Synchronization Checking Protocol and VME board Header word

K. Ohl
Yale Univ.

J. Wahl , P. Wilson
Univ. of Chicago

1 Introduction

In this note we specify a standard protocol for checking synchronization for use on all frontend and trigger systems in the CDF Run II upgrade. It involves a bunch counter to time stamp the data which is reset using the Bunch Zero signal from the Tevatron. The purpose of the time stamp is to aid in synchronizing different boards within a given subsystem and to synchronize the various subsystems of the frontend and trigger. Once the system is setup it can be used to check that all data in the event readout stream are from the same crossing. The contents of the bunch counter will be written into the event stream in a header word which is also specified in this note.

2 Bunch Counting Protocol

1. Each Frontend and L1 Trigger board shall have an 8 bit bunch counter.

2. The L1 Pipeline/FIFO and the bunch counter should both be clocked using the 132nsec CDF_CLK. The CDF_CLK signal is available on the P2 backplane of the CDF 9U VME crates[1]. For the purposes of this counter the CDF_CLK should *not* be gated by the Bunch Crossing signal.

3. Frontend and L1 trigger cards will latch the counter into a L1 FIFO/pipeline when they store other data in L1 FIFOs/Pipelines. On a L1 accept the contents of the counters FIFO/Pipeline will be stored in the appropriate L2 buffer (1 of 4) which will be read out on a L2 accept.

4. The counter shall be reset on a signal derived from the Bunch zero signal so as to tag the data on all boards with the number of crossings since Bunch Zero collided in B0. This will require an offset be applied on each board either to the reset pulse or to the stored data. This offset will correspond to a few crossings for frontend cards, be larger for L1 primitive boards and largest for FRED (nearly 42). For maximum flexibility it is strongly advised that this offset be programmable.

5. L1 systems which provide primitives to L2 should send the bunch counter with the primitives to the L2 processors. Level 2 can then write write the counter values with it's data.

6. All boards should write the contents of the bunch counter into the event stream in a 32 bit board header word. The header word will be specified below.

Once the system is setup and running all boards should have the same value for the time stamp stored for a given event. A board or boards which have a different value will be an indication of loss of synchronization.

During commissioning the offsets on each card can be set to 0. Then the difference between the value of the counters can be used to study the delays between systems. Even at this stage all boards within a system should have the same value in the counter.

3 Board Header Word Specification

The board header word will have 32 bits consisting of a 24 bit board ID and the 8 bit time stamp specified above. The allocation of the 32 bits is given in Table 1. Note that bits 8-31 will be the same for every event from a given board but that bits 0-7 will have to come from 1 of 4 L2 buffers.

The board header word should be located in the first L2 Buffer address for each of the 4 L2 buffers (YY080000, YY090000, YY0A0000 and YY0B0000 respectively [2]). In the data stream the TRACER will insert a header word for the crate. Each board will then have it's own header word followed by it's data.

Bit	Description
0-7	Bunch ID: 8 Bit counter from Bunch Zero
8-12	Geographical Address - 5 bits
13-22	Board Serial Number - 10 bits
23-31	Board Type - 9 bits

Table 1: Board Header Word Specification

There will be a board type number Czar (as yet unnamed) who will allocate board type numbers. The serial numbers are to be allocated by the boards designers.

References

[1] T. Shaw and G.Sullivan, *A CDF standard VME readout crate for the Upgrade*, CDF/DOC/TRIGGER/CDFR/2388, 1993.

[2] T. Shaw and W. Stuermer, *Designer's Guide fot Modules to go into the CDF Custom Backplane.*