SN54LS670 . . . J OR W PACKAGE
SN74LS670 . . . D OR N PACKAGE

(TOP VIEW)

D2 1 18 VCC
D3 2 15 Q1
D4 3 14 WA
RB 4 12 WB
RA 5 12 GW
Q4 6 11 Q1
Q3 7 10 Q1
GND 8 5 Q2

SN54LS670 . . . FK PACKAGE
(TOP VIEW)

D4 4 18 WA
RB 5 17 WB
NC 6 16 NC
RA 7 15 GW
Q4 8 14 Q1
GND 9 12 NC
Z1 10 13 NC
Z2 2 12 NC
Z3 3 11 NC

NC — No internal connection.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, GW, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, GR, is high, the data outputs are inhibited and go into the high-impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the output terminals.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 nanoseconds typical) and the read time (24 nanoseconds typical). The register file has a nondestructive readout so data is not lost when addressed.

All inputs except read enable and write enable are buffered to lower the drive requirements to one Series 54LS/74LS standard load, and input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and have high-sink-current, three-state outputs. Up to 128 of these outputs may be bus connected for increasing the capacity up to 512 words. Any number of these registers may be paralleled to provide n-bit word length.

The SN54LS670 is characterized for operation over the full military temperature range of −55 °C to 125 °C; the SN74LS670 is characterized for operation from 0 °C to 70 °C.
SN54LS670, SN74LS670
4-BY-4 REGISTER FILES WITH 3-OUTPUTS

logic symbol

RAM 4x4

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

<table>
<thead>
<tr>
<th>WRITE INPUTS</th>
<th>WRITE Q0</th>
<th>WRITE Q1</th>
<th>WRITE Q2</th>
<th>WRITE Q3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wb</td>
<td>Wa</td>
<td>Wy</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>0 = 0</td>
<td>0 = 0</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>0 = 0</td>
<td>0 = 0</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>0 = 0</td>
<td>0 = 0</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>0 = 0</td>
<td>0 = 0</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>H</td>
<td>0 = 0</td>
<td>0 = 0</td>
</tr>
</tbody>
</table>

READ FUNCTION TABLE (SEE NOTES A AND D)

<table>
<thead>
<tr>
<th>READ INPUTS</th>
<th>READ Q1</th>
<th>READ Q2</th>
<th>READ Q3</th>
<th>READ Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rb</td>
<td>Ra</td>
<td>Rry</td>
<td>Q1</td>
<td>Q2</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>W0B1</td>
<td>W0B2</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>W1B1</td>
<td>W1B2</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>W2B1</td>
<td>W2B2</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>W3B1</td>
<td>W3B2</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>H</td>
<td>Z</td>
<td>Z</td>
</tr>
</tbody>
</table>

NOTES:
A. H = high level, L = low level, X = irrelevant, Z = high impedance (off)
B. (C) = (D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. Q0 = 0 before the indicated input conditions were established.
D. W0B1 = The first bit of word 0, etc.

schematics of inputs and outputs

TYPICAL OF ALL OUTPUTS

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logic diagram (positive logic)

Pins numbers shown are for D, J, N, and W packages.
### SN54LS670, SN74LS670
### 4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

- **Supply voltage, VCC (see Note 1)**: 7 V
- **Input voltage**: 7 V
- **Off-state output voltage**: 5.5 V
- **Operating free-air temperature range**: SN54LS670: -55°C to 125°C, SN74LS670: 0°C to 70°C
- **Storage temperature range**: -65°C to 150°C

### recommended operating conditions

<table>
<thead>
<tr>
<th></th>
<th>SN54LS670</th>
<th>SN74LS670</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, VCC</td>
<td>4.5</td>
<td>5.5</td>
<td>5.25 V</td>
</tr>
<tr>
<td>High-level output current, I_{OH}</td>
<td>-1</td>
<td>-2.6 mA</td>
<td></td>
</tr>
<tr>
<td>Low-level output current, I_{OL}</td>
<td>4 mA</td>
<td>8 mA</td>
<td></td>
</tr>
<tr>
<td>Setup times, high- or low-level data (see Figure 2)</td>
<td>Data input with respect to write enable, t_{WU}(D)</td>
<td>10 ns</td>
<td>10 ns</td>
</tr>
<tr>
<td></td>
<td>Write select with respect to write enable, t_{WU}(W)</td>
<td>16 ns</td>
<td>15 ns</td>
</tr>
<tr>
<td>Hold times, high- or low-level data (see Note 2 and Figure 2)</td>
<td>Data input with respect to write enable, t_{WH}(D)</td>
<td>15 ns</td>
<td>15 ns</td>
</tr>
<tr>
<td></td>
<td>Write select with respect to write enable, t_{WH}(W)</td>
<td>5 ns</td>
<td>5 ns</td>
</tr>
<tr>
<td>Latch time for new data, t_{LATCH} (see Note 3)</td>
<td>26 ns</td>
<td>25 ns</td>
<td>ns</td>
</tr>
<tr>
<td>Operating free-air temperature range, T_{A}</td>
<td>-55°C</td>
<td>126°C</td>
<td>0°C to 70°C</td>
</tr>
</tbody>
</table>

**NOTES:**

1. Voltage values are with respect to network ground terminal.
2. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, t_{WU}(W) can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during t_{WH}(W) will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.
3. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.
### Electrical Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>SN54LS670</th>
<th>SN74LS670</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
</tr>
<tr>
<td>V_{IH} - High-level input voltage</td>
<td>V_{CC} = MIN, I_{I} = -18 mA</td>
<td>2.4</td>
<td>2.4</td>
</tr>
<tr>
<td>V_{IL} - Low-level input voltage</td>
<td>V_{CC} = MIN, I_{I} = -18 mA</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>V_{IH} - High-level output voltage</td>
<td>V_{CC} = MIN, I_{O} = -1 mA</td>
<td>2.4</td>
<td>4.0</td>
</tr>
<tr>
<td>V_{IL} - Low-level output voltage</td>
<td>V_{CC} = MIN, I_{O} = -2.6 mA</td>
<td>2.4</td>
<td>4.0</td>
</tr>
<tr>
<td>I_{OZH} - Off-state output current, high-level voltage applied</td>
<td>V_{CC} = MAX, V_{I} = 2 V, V_{O} = 2.7 V</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>I_{OZH} - Off-state output current, low-level voltage applied</td>
<td>V_{CC} = MAX, V_{I} = 2 V, V_{O} = 0.4 V</td>
<td>-20</td>
<td>-20</td>
</tr>
<tr>
<td>I_{L} - Input current at maximum input voltage</td>
<td>V_{CC} = MAX, V_{I} = 7 V</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>I_{IH} - High-level input current</td>
<td>V_{CC} = MAX, V_{I} = 2.7 V</td>
<td>0.7</td>
<td>0.7</td>
</tr>
<tr>
<td>I_{IL} - Low-level input current</td>
<td>V_{CC} = MAX, V_{I} = 0.4 V</td>
<td>0.3</td>
<td>0.3</td>
</tr>
<tr>
<td>I_{OS} - Short-circuit current</td>
<td>V_{CC} = MAX, See Note 4</td>
<td>-30</td>
<td>-30</td>
</tr>
<tr>
<td>I_{CC} - Supply current</td>
<td>V_{CC} = MAX, See Note 4</td>
<td>30</td>
<td>50</td>
</tr>
</tbody>
</table>

---

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2. All typical values are at V_{CC} = 5 V, T_{A} = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
4. Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.6 V is applied to all data inputs and both enable inputs, all address inputs are grounded and all outputs are open.

### Switching Characteristics, V_{CC} = 5 V, T_{A} = 25°C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>From (Input)</th>
<th>To (Output)</th>
<th>Test Conditions</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>T_{PLL}</td>
<td>Read select</td>
<td>Any Q</td>
<td>V_{CC} = 15 pF, R_{L} = 2 kΩ</td>
<td>23</td>
<td>40</td>
<td>ns</td>
</tr>
<tr>
<td>T_{PH}</td>
<td>Write enable</td>
<td>Any Q</td>
<td>V_{CC} = 15 pF, R_{L} = 2 kΩ</td>
<td>26</td>
<td>45</td>
<td>ns</td>
</tr>
<tr>
<td>T_{PL}</td>
<td>Data</td>
<td>Any Q</td>
<td>V_{CC} = 15 pF, R_{L} = 2 kΩ</td>
<td>22</td>
<td>40</td>
<td>ns</td>
</tr>
<tr>
<td>T_{PH}</td>
<td>Read enable</td>
<td>Any Q</td>
<td>V_{CC} = 15 pF, R_{L} = 2 kΩ</td>
<td>16</td>
<td>35</td>
<td>ns</td>
</tr>
</tbody>
</table>

---

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SN54LS670, SN74LS670
4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION

NOTES:
A. \( C_L \) includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.

LOAD CIRCUIT

FIGURE 1

WRITE SELECT
INPUT \( W_A \) or \( W_B \)
(See Note A)

DATA INPUT
\( D_1, D_2, D_3, \) or \( D_4 \)
(See Note A)

WRITE ENABLE
INPUT \( G_W \)

READ SELECT
INPUT \( R_A \) or \( R_B \)
(See Note B)

OUTPUT
\( Q_1, Q_2, Q_3, \) or \( Q_4 \)

VOLTAGE WAVEFORMS (\( S_1 \) AND \( S_2 \) ARE CLOSED)

NOTES:
A. High-level input pulses at the select and data inputs are illustrated; however, times associated with low-level pulses are measured from the same reference points.
B. When measuring delay times from a read select input, the read-enable input is low.
C. Input waveforms are supplied by generators having the following characteristics: \( f_{\text{out}} \leq 2 \text{ MHz}, \ Z_{\text{out}} \leq 50 \Omega, \) duty cycle \( \leq 50\%, \) \( t_r \leq 15 \text{ ns}, t_f \leq 6 \text{ ns}. \)

FIGURE 2

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PARAMETER MEASUREMENT INFORMATION

DATA INPUT
D1, D2, D3, or D4

WRITE ENABLE
INPUT GW

OUTPUT
Q1, Q2, Q3, or Q4

VOLTAGE WAVEFORM 1 (S1 AND S2 ARE CLOSED)

DATA INPUT
D1, D2, D3, or D4

WRITE ENABLE
INPUT GW

OUTPUT
Q1, Q2, Q3, or Q4

VOLTAGE WAVEFORM 2 (S1 AND S2 ARE CLOSED)

NOTES:
A. Each select address is tested. Prior to the start of each of the above tests both write and read address inputs are stabilized with \( W_A = W_B = W_G \). During the test, \( G_R \) is low.
B. Input waveforms are supplied by generators having the following characteristics: \( P_{RR} < 1 \text{ MHz}, Z_{out} = 50 \text{ \Omega} \), duty cycle \( < 50\% \),
\( t_r \leq 15 \text{ ns}, t_f \leq 6 \text{ ns} \).

FIGURE 3

READ ENABLE

WAVEFORM 1
(See Note A)

WAVEFORM 2
(See Note A)

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES:
A. Waveforms 1 is for an output with internal conditions such that the output is low except when disabled by the read-enable input. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the read-enable input.
B. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.
C. Input waveforms are supplied by generators having the following characteristics: \( P_{RR} < 1 \text{ MHz}, Z_{out} = 50 \text{ \Omega} \), duty cycle \( < 50\% \),
\( t_r \leq 15 \text{ ns}, t_f \leq 6 \text{ ns} \).

FIGURE 4
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