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J3 Backplane and Transition Module (L1AUX) for the Level 1 Calorimeter Trigger Upgrade

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1 Introduction

The Level 1 calorimeter crates for the trigger upgrade will be 9U VME crates as per the standard for the CDF upgrade[1]. Each Level 1 calorimeter crate has 16 DIRAC boards, 2 CRATESUM boards and 2 boards for interface to the DAQ system trigger supervisor. A custom J3 backplane will be used to transmit the outputs from DIRAC[2] to the CRATE SUM board [3]. Input data from the front-end crates is received by 16 transition modules (L1AUX), one for each DIRAC board, and is directed via feedthrough pins on the J3 backplane to the DIRAC boards.

This note has been revised to use 220 pin 2mm Hard Metric connectors on all slots. In addition the J3 backplane is also planned to be used for the L1 Decision crate.

2 J3 Backplane

The 16 DIRAC boards use slots 4-7, 9-15 and 17-21 and the 2 CRATESUM boards use slots 8 and 16 of the Level 1 calorimetry crate. The 16 AUX boards plug into the rear of the crate behind each of the DIRAC boards. All of these boards have connectors labeled P3 which make connection to the J3 backplane. Slots 1-3 of the crate are reserved for DAQ modules and have no connectors on the J3 backplane. Signal routing on the J3 backplane is divided into two identical halves each centered around a Cratesum board (slots 8 and 16). All signals are contained completely on a half backplane while the ground planes cover the whole board. All signals are point to point with a maximum distance of 4 VME slots.

2.1 L1 Calorimetery Signal Definitions

The signals using the P3 connector of DIRAC consist of inputs from the DIRAC auxiliary board and output data to the Cratesum board. Table 1 gives the pin assignments for the DIRAC connectors. There are 12 input data words from the AUX board with signals labeled TOWINxx(0:9) for trigger tower xx bits 0:11. There are 24 bits of output data from DIRAC to the cratesum board: TRSUM(0:15) and ETSUM(0:7). A total of 146 signal and power pins are provided by a 220 pin 2mm hard metric connector with 5 columns of 44 pins each.

All pins feedthrough the backplane connecting to DIRAC and the AUX receiver board. Two additional pins are provided for control from DIRAC to the AUX card.

Each Cratesum board receives 24 bits of data from each of the 8 DIRAC boards in its half crate. Table 2 gives the pin assignments for the 2 Cratesum slots. The signals are labeled TRSUMxx(0:15) for the trigger summary words and ETSUMxx(0:7) for the ΣE_T words where xx is the number of the DIRAC board in the half crate. The 192 signals are handled by a 220 pin 2mm hard metric (e.g. AMP Z-pack) connector with 5 columns of 44 pins each.

2.2 L1 Decision Signal Definitions

The same J3 Backplane design will be used for the L1 Decision crate. In this crate the PreFRED modules will occupy slots used for DIRAC cards and FRED will occupy the a Cratesum slot (and possibly the adjacent slot). Table 3 lists the pinout for the PreFRED slots and Table 4 lists the pinout for the FRED slot.

2.3 Construction

There are 4 signal layers using 1 oz copper and 7mil traces. The maximum trace length is approximately 5 inches. The maximum current flowing in a trace will be 60 mAmp. There are two ground planes, one between each of the two pairs of signal layers. The PC board thickness will be 0.125". Rear shrouds will be selected to be compatible with the CDF VIPA crate J1-J0-J2 backplane.

3 Auxiliary Receiver Board (L1AUX)

The receiver board is a 9U by 120 mm transition module which terminates the trigger cables from the front-end (ADMEM) boards. It receives the differential signals, converts them to single-ended and passes them through the P3 connector the DIRAC card. Since each DIRAC card handles 12 trigger towers, the L1AUX card must handle 12 input cables fom the ADMEM boards. For each Central DIRAC board, an additional input is needed from the Wall Hadron to cover the overlap region between CHA and WHA. This additional input is then summed with the appropriate CHA channel to provide 12 outputs to DIRAC. The input channels are number 0-11 with 7a being used for the 13th input from the WHA on Central boards.

3.1 Input Signals

The signals from front end boards consist of 13 separate 10 bit words transmitted differentially on a 20 conductor twisted pair cable wrapped with a ground shield. Each transition board receives 13 cables using 20 pin SCSI-II type connectors. The pin assignment of these connectors is listed in Table 5. Each twisted pair is terminated in approximately 140 Ω with a center tap of 29.5 Ω which is capacatively coupled back to the cable ground shield. The ground of each cable can also be terminated frough and RC network to the local board ground. National DS90C31AT LVDS differential drivers are used on the front-end boards and DS90C32AT receivers are used on the L1AUX boards. These are low power CMOS chips satisfying LVDS standards.

3.2 Endwall Summing

The summing of input channels 7 and 7a is carried out by an Altera 7032 EPLD. The chip is programmed to sum two 10 bit words into a single 10 bit out with all bits enabled on an overflow. For use in the Plug or the L1 Decision crate the summing can be disabled and the data from channel 7 is sent through a buffer directly to DIRAC. The summing or pass through mode is selected by the AUX_SUM_EN control signal which is fed through the J3 backplane from a register on DIRAC. A spare control signal (AUX_SPARE) is also routed for future use.

3.3 Output to DIRAC

The receiver outputs are transmitted single ended through the P3 connector to the DIRAC board. The P3 connecter pin assignments are the same as for the DIRAC board and are listed in Table 1. The signals ETSUM and TRSUM have no connection on the transition module.

3.4 Power and Indicators

Power required is approximately 750mA from the +5V power supply (running at 7 MHz). Power and return connections will be provided by the P0 connector with a top side ground shield. The P2 connector is required for alignment purposes and might not be provided with connections to power and ground if the space is needed for signal routing. The +5V supply will be fused at 1.5A and have a transient supressor (Motorola 1N5708). Two LED indicators will be provided on the rear panel showing the state of the +5V supply and the state of the AUX_SUM_EN bit.

3.5 Mechanics

The PCB consists of 4 signals layers with 7 mil traces, a +5V power plane and a single ground plane. Overall thickness is 0.062" to allow complete insertion of pins on the input connectors. Seven of the input connectors must be mounted inboard and are set on nylon washers for proper alignment. All input connectors will be mounted with star washers to ensure good contact between the connector shell (sheild) and the board termination network. A frontpanel will be used but must be made of an inulating material to avoid electrical contact with the input connector shells. A board stiffener of Fermilab design ("9U VME Board Stiffener" Drawing WS-9USTIF-032597) will be mounted vertically 0.25" from the P0-P2-P3 connectors.

References

[1] G. Sullivan and T. Shaw, *A Standard Front-end and Trigger VME Readout Crate for the CDF Upgrade*, CDF/TRIGGER/DOC/CDFR/2388, (1994).

[2] J. Wahl, *DIRAC - The Final Specification*, CDF/TRIGGER/DOC/4425 (1997).

[3] D. Toback, *Crate Sum - Upgrade for Run II*, CDF Trigger note TGN-91, (1993).

Table 1: Pin assignments for DIRAC and Receiver P3 connectors (J3 Backplane). The Receiver board makes no connection to the TRSUM or ETSUM pins. The numbers in parentheses are the bit numbers with 0 as least significant. The xx in TOWINxx(0:9) represents the channel number with channel 0 having the lowest η and channel 11 the highest.

	Row						
Pin #	z	a	b	c	d	e	f
1	GND	GND	TRSUM(0)	TRSUM(1)	TRSUM(2)	TRSUM(3)	GND
2	GND	N/C	TRSUM(4)	TRSUM(5)	GND	TRSUM(6)	GND
3	GND	N/C	TRSUM(7)	GND	TRSUM(8)	TRSUM(9)	GND
4	GND	N/C	TRSUM(10)	TRSUM(11)	GND	TRSUM(12)	GND
5	GND	GND	TRSUM(13)	GND	TRSUM(14)	TRSUM(15)	GND
6	GND	N/C	TOWIN0(0)	TOWIN0(1)	TOWIN0(2)	TOWIN0(3)	GND
7	GND	N/C	TOWIN0(4)	TOWIN0(5)	GND	TOWIN0(6)	GND
8	GND	N/C	TOWIN0(7)	TOWIN0(8)	TOWIN0(9)	TOWIN1(0)	GND
9	GND	GND	TOWIN1(1)	GND	TOWIN1(2)	TOWIN1(3)	GND
10	GND	N/C	TOWIN1(4)	TOWIN1(5)	TOWIN1(6)	TOWIN1(7)	GND
11	GND	N/C	TOWIN1(8)	TOWIN1(9)	GND	TOWIN2(0)	GND
12	GND	N/C	TOWIN2(1)	TOWIN2(2)	TOWIN2(3)	TOWIN2(4)	GND
13	GND	GND	TOWIN2(5)	GND	TOWIN2(6)	TOWIN2(7)	GND
14	GND	N/C	TOWIN2(8)	TOWIN2(9)	TOWIN3(0)	TOWIN3(1)	GND
15	GND	N/C	TOWIN3(2)	TOWIN3(3)	GND	TOWIN3(4)	GND
16	GND	N/C	TOWIN3(5)	TOWIN3(6)	TOWIN3(7)	TOWIN3(8)	GND
17	GND	GND	TOWIN3(9)	GND	TOWIN4(0)	TOWIN4(1)	GND
18	GND	N/C	TOWIN4(2)	TOWIN4(3)	TOWIN4(4)	TOWIN4(5)	GND
19	GND	N/C	TOWIN4(6)	TOWIN4(7)	GND	TOWIN4(8)	GND
20	GND	N/C	TOWIN4(9)	TOWIN5(0)	TOWIN5(1)	TOWIN5(2)	GND
21	GND	GND	TOWIN5(3)	GND	TOWIN5(4)	TOWIN5(5)	GND
22	GND	N/C	TOWIN5(6)	TOWIN5(7)	TOWIN5(8)	TOWIN5(9)	GND
23	GND	N/C	TOWIN6(0)	TOWIN6(1)	GND	TOWIN6(2)	GND
24	GND	N/C	TOWIN6(3)	TOWIN6(4)	TOWIN6(5)	TOWIN6(6)	GND
25	GND	GND	TOWIN6(7)	GND	TOWIN6(8)	TOWIN6(9)	GND
26	GND	N/C	TOWIN7(0)	TOWIN7(1)	TOWIN7(2)	TOWIN7(3)	GND
27	GND	N/C	TOWIN7(4)	TOWIN7(5)	GND	TOWIN7(6)	GND
28	GND	N/C	TOWIN7(7)	TOWIN7(8)	TOWIN7(9)	TOWIN8(0)	GND
29	GND	GND	TOWIN8(1)	GND	TOWIN8(2)	TOWIN8(3)	GND
30	GND	N/C	TOWIN8(4)	TOWIN8(5)	TOWIN8(6)	TOWIN8(7)	GND
31	GND	N/C	TOWIN8(8)	TOWIN8(9)	GND	TOWIN9(0)	GND
32	GND	N/C	TOWIN9(1)	TOWIN9(2)	TOWIN9(3)	TOWIN9(4)	GND
33	GND	GND	TOWIN9(5)	GND	TOWIN9(6)	TOWIN9(7)	GND
Connector Key (equivalent to 3 pins)							
34	GND	N/C	TOWIN9(8)	TOWIN9(9)	TOWIN10(0)	TOWIN10(1)	GND
35	GND	N/C	TOWIN10(2)	TOWIN10(3)	GND	TOWIN10(4)	GND
36	GND	N/C	TOWIN10(5)	TOWIN10(6)	TOWIN10(7)	TOWIN10(8)	GND
37	GND	GND	TOWIN10(9)	GND	TOWIN11(0)	TOWIN11(1)	GND
38	GND	N/C	TOWIN11(2)	TOWIN11(3)	TOWIN11(4)	TOWIN11(5)	GND
39	GND	N/C	TOWIN11(6)	TOWIN11(7)	GND	TOWIN11(8)	GND
40	GND	N/C	TOWIN11(9)	AUX_SUM_EN	ETSUM(0)	ETSUM(1)	GND
41	GND	GND	ETSUM(2)	AUX_SPARE	ETSUM(3)	ETSUM(4)	GND
42	GND	N/C	ETSUM(5)	ETSUM(6)	GND	ETSUM(7)	GND
43	GND	N/C	N/C	AUX_ENABLE	N/C	N/C	GND
44	GND	N/C	N/C	N/C	N/C	N/C	GND

Table 2: Pin assignments for the CRATESUM P3 connector (J3 Backplane). The number at the end of the signal name is the DIRAC board within the half crate from which the signal came. The number in parentheses is the bit number with 0 as least significant.

Pin #	z	a	b	c	d	e	f
1	GND	TRSUM0(2)	TRSUM0(1)	TRSUM0(0)	TRSUM7(1)	TRSUM7(0)	GND
2	GND	TRSUM0(4)	TRSUM0(3)	GND	TRSUM7(3)	TRSUM7(2)	GND
3	GND	TRSUM0(7)	TRSUM0(6)	TRSUM0(5)	TRSUM7(5)	TRSUM7(4)	GND
4	GND	TRSUM0(9)	TRSUM0(8)	GND	TRSUM7(7)	TRSUM7(6)	GND
5	GND	TRSUM0(11)	TRSUM0(10)	TRSUM7(10)	TRSUM7(9)	TRSUM7(8)	GND
6	GND	TRSUM0(13)	TRSUM0(12)	GND	TRSUM7(12)	TRSUM7(11)	GND
7	GND	TRSUM0(15)	TRSUM0(14)	TRSUM7(15)	TRSUM7(14)	TRSUM7(13)	GND
8	GND	TRSUM1(2)	TRSUM1(1)	TRSUM1(0)	TRSUM6(1)	TRSUM6(0)	GND
9	GND	TRSUM1(4)	TRSUM1(3)	GND	TRSUM6(3)	TRSUM6(2)	GND
10	GND	TRSUM1(7)	TRSUM1(6)	TRSUM1(5)	TRSUM6(5)	TRSUM6(4)	GND
11	GND	TRSUM1(9)	TRSUM1(8)	GND	TRSUM6(7)	TRSUM6(6)	GND
12	GND	TRSUM1(11)	TRSUM1(10)	TRSUM6(10)	TRSUM6(9)	TRSUM6(8)	GND
13	GND	TRSUM1(13)	TRSUM1(12)	GND	TRSUM6(12)	TRSUM6(11)	GND
14	GND	TRSUM1(15)	TRSUM1(14)	TRSUM6(15)	TRSUM6(14)	TRSUM6(13)	GND
15	GND	TRSUM2(2)	TRSUM2(1)	TRSUM2(0)	TRSUM5(1)	TRSUM5(0)	GND
16	GND	TRSUM2(4)	TRSUM2(3)	GND	TRSUM5(3)	TRSUM5(2)	GND
17	GND	TRSUM2(7)	TRSUM2(6)	TRSUM2(5)	TRSUM5(5)	TRSUM5(4)	GND
18	GND	TRSUM2(9)	TRSUM2(8)	GND	TRSUM5(7)	TRSUM5(6)	GND
19	GND	TRSUM2(11)	TRSUM2(10)	TRSUM5(10)	TRSUM5(9)	TRSUM5(8)	GND
20	GND	TRSUM2(13)	TRSUM2(12)	GND	TRSUM5(12)	TRSUM5(11)	GND
21	GND	TRSUM2(15)	TRSUM2(14)	TRSUM5(15)	TRSUM5(14)	TRSUM5(13)	GND
22	GND	TRSUM3(2)	TRSUM3(1)	TRSUM3(0)	TRSUM4(1)	TRSUM4(0)	GND
23	GND	TRSUM3(4)	TRSUM3(3)	GND	TRSUM4(3)	TRSUM4(2)	GND
24	GND	TRSUM3(7)	TRSUM3(6)	TRSUM3(5)	TRSUM4(5)	TRSUM4(4)	GND
25	GND	TRSUM3(9)	TRSUM3(8)	GND	TRSUM4(7)	TRSUM4(6)	GND
26	GND	TRSUM3(11)	TRSUM3(10)	TRSUM4(10)	TRSUM4(9)	TRSUM4(8)	GND
27	GND	TRSUM3(13)	TRSUM3(12)	GND	TRSUM4(12)	TRSUM4(11)	GND
28	GND	TRSUM3(15)	TRSUM3(14)	TRSUM4(15)	TRSUM4(14)	TRSUM4(13)	GND
29	GND	GND	GND	GND	GND	GND	GND
30	GND	ETSUM3(1)	ETSUM3(0)	GND	ETSUM4(1)	ETSUM4(0)	GND
31	GND	ETSUM3(3)	ETSUM3(2)	GND	ETSUM4(3)	ETSUM4(2)	GND
32	GND	ETSUM3(5)	ETSUM3(4)	ETSUM4(6)	ETSUM4(5)	ETSUM4(4)	GND
33	GND	ETSUM3(7)	ETSUM3(6)	GND	ETSUM5(0)	ETSUM4(7)	GND
Connector Key (equivalent to 3 pins)							
34	GND	ETSUM2(1)	ETSUM2(0)	GND	ETSUM5(2)	ETSUM5(1)	GND
35	GND	ETSUM2(3)	ETSUM2(2)	GND	ETSUM5(4)	ETSUM5(3)	GND
36	GND	ETSUM2(6)	ETSUM2(5)	ETSUM2(4)	ETSUM5(6)	ETSUM5(5)	GND
37	GND	ETSUM1(0)	ETSUM2(7)	GND	ETSUM6(0)	ETSUM5(7)	GND
38	GND	ETSUM1(2)	ETSUM1(1)	GND	ETSUM6(2)	ETSUM6(1)	GND
39	GND	ETSUM1(4)	ETSUM1(3)	GND	ETSUM6(4)	ETSUM6(3)	GND
40	GND	ETSUM1(6)	ETSUM1(5)	ETSUM6(7)	ETSUM6(6)	ETSUM6(5)	GND
41	GND	ETSUM0(0)	ETSUM1(7)	GND	ETSUM7(1)	ETSUM7(0)	GND
42	GND	ETSUM0(2)	ETSUM0(1)	GND	ETSUM7(3)	ETSUM7(2)	GND
43	GND	ETSUM0(4)	ETSUM0(3)	GND	ETSUM7(5)	ETSUM7(4)	GND
44	GND	ETSUM0(7)	ETSUM0(6)	ETSUM0(5)	ETSUM7(7)	ETSUM7(6)	GND

Table 3: Pin assignments for the PreFRED-J3 Backplane connection. TRIGBIT = output trigger bits to FRED, CSIN = input from CRATESUM, L1 Muon system or XTRP. In the case of the SUMET board, only the four least significant TRIGBITs are used, and the CSIN pins transmit the wedge transverse energies. In the case of the TOWTRG module, CSIN brings in trigger bits. The index associated with CSIN represents the channel number. The numbers in parentheses are the bit numbers with 0 as least significant. AUX_SUM_EN is connected to ground on the board so as to forbid the summing of channels enabled for DIRAC. The Receiver Aux-card makes no connection to the TRIGBIT pins.

	Row						
Pin #	z	a	b	c	d	e	f
1	GND	GND	TRIGBIT(0)	TRIGBIT(1)	TRIGBIT(2)	TRIGBIT(3)	GND
2	GND	N/C	TRIGBIT(4)	TRIGBIT(5)	GND	TRIGBIT(6)	GND
3	GND	N/C	TRIGBIT(7)	GND	TRIGBIT(8)	TRIGBIT(9)	GND
4	GND	N/C	TRIGBIT(10)	TRIGBIT(11)	GND	TRIGBIT(12)	GND
5	GND	GND	TRIGBIT(13)	GND	TRIGBIT(14)	TRIGBIT(15)	GND
6	GND	N/C	CSIN0(0)	CSIN0(1)	CSIN0(2)	CSIN0(3)	GND
7	GND	N/C	CSIN0(4)	CSIN0(5)	GND	CSIN0(6)	GND
8	GND	N/C	CSIN0(7)	CSIN0(8)	CSIN0(9)	CSIN1(0)	GND
9	GND	GND	CSIN1(1)	GND	CSIN1(2)	CSIN1(3)	GND
10	GND	N/C	CSIN1(4)	CSIN1(5)	CSIN1(6)	CSIN1(7)	GND
11	GND	N/C	CSIN1(8)	CSIN1(9)	GND	CSIN2(0)	GND
12	GND	N/C	CSIN2(1)	CSIN2(2)	CSIN2(3)	CSIN2(4)	GND
13	GND	GND	CSIN2(5)	GND	CSIN2(6)	CSIN2(7)	GND
14	GND	N/C	CSIN2(8)	CSIN2(9)	CSIN3(0)	CSIN3(1)	GND
15	GND	N/C	CSIN3(2)	CSIN3(3)	GND	CSIN3(4)	GND
16	GND	N/C	CSIN3(5)	CSIN3(6)	CSIN3(7)	CSIN3(8)	GND
17	GND	GND	CSIN3(9)	GND	CSIN4(0)	CSIN4(1)	GND
18	GND	N/C	CSIN4(2)	CSIN4(3)	CSIN4(4)	CSIN4(5)	GND
19	GND	N/C	CSIN4(6)	CSIN4(7)	GND	CSIN4(8)	GND
20	GND	N/C	CSIN4(9)	CSIN5(0)	CSIN5(1)	CSIN5(2)	GND
21	GND	GND	CSIN5(3)	GND	CSIN5(4)	CSIN5(5)	GND
22	GND	N/C	CSIN5(6)	CSIN5(7)	CSIN5(8)	CSIN5(9)	GND
23	GND	N/C	CSIN6(0)	CSIN6(1)	GND	CSIN6(2)	GND
24	GND	N/C	CSIN6(3)	CSIN6(4)	CSIN6(5)	CSIN6(6)	GND
25	GND	GND	CSIN6(7)	GND	CSIN6(8)	CSIN6(9)	GND
26	GND	N/C	CSIN7(0)	CSIN7(1)	CSIN7(2)	CSIN7(3)	GND
27	GND	N/C	CSIN7(4)	CSIN7(5)	GND	CSIN7(6)	GND
28	GND	N/C	CSIN7(7)	CSIN7(8)	CSIN7(9)	CSIN8(0)	GND
29	GND	GND	CSIN8(1)	GND	CSIN8(2)	CSIN8(3)	GND
30	GND	N/C	CSIN8(4)	CSIN8(5)	CSIN8(6)	CSIN8(7)	GND
31	GND	N/C	CSIN8(8)	CSIN8(9)	GND	CSIN9(0)	GND
32	GND	N/C	CSIN9(1)	CSIN9(2)	CSIN9(3)	CSIN9(4)	GND
33	GND	GND	CSIN9(5)	GND	CSIN9(6)	CSIN9(7)	GND
Connector Key (equivalent to 3 pins)							
34	GND	N/C	CSIN9(8)	CSIN9(9)	CSIN10(0)	CSIN10(1)	GND
35	GND	N/C	CSIN10(2)	CSIN10(3)	GND	CSIN10(4)	GND
36	GND	N/C	CSIN10(5)	CSIN10(6)	CSIN10(7)	CSIN10(8)	GND
37	GND	GND	CSIN10(9)	GND	CSIN11(0)	CSIN11(1)	GND
38	GND	N/C	CSIN11(2)	CSIN11(3)	CSIN11(4)	CSIN11(5)	GND
39	GND	N/C	CSIN11(6)	CSIN11(7)	GND	CSIN11(8)	GND
40	GND	N/C	CSIN11(9)	AUX_SUM_EN	TRIGBIT(16)	TRIGBIT(17)	GND
41	GND	GND	TRIGBIT(18)	AUX_SPARE	TRIGBIT(19)	B0_DELAYED	GND
42	GND	N/C	BP_SPARE(0)	BP_SPARE(1)	GND	BP_SPARE(2)	GND
43	GND	N/C	N/C	AUX_ENABLE	N/C	N/C	GND
44	GND	N/C	N/C	N/C	N/C	N/C	GND

Table 4: Pin assignments for the FRED P3 connector (J3 Backplane). The number at the end of the signal name is the PreFRED board within the half crate from which the signal came. The number in parentheses is the bit number with 0 as least significant. Signals labeled ~~TRIGBIT~~ are not connected on the FRED module but do have a connection on the backplane.

Pin #	z	a	b	c	d	e	f
1	GND	TRIGBIT0(2)	TRIGBIT0(1)	TRIGBIT0(0)	TRIGBIT7(1)	TRIGBIT7(0)	GND
2	GND	~~TRIGBIT~~0(4)	TRIGBIT0(3)	GND	TRIGBIT7(3)	TRIGBIT7(2)	GND
3	GND	~~TRIGBIT~~0(7)	~~TRIGBIT~~0(6)	~~TRIGBIT~~0(5)	TRIGBIT7(5)	TRIGBIT7(4)	GND
4	GND	~~TRIGBIT~~0(9)	~~TRIGBIT~~0(8)	GND	TRIGBIT7(7)	TRIGBIT7(6)	GND
5	GND	~~TRIGBIT~~0(11)	~~TRIGBIT~~0(10)	TRIGBIT7(10)	TRIGBIT7(9)	TRIGBIT7(8)	GND
6	GND	~~TRIGBIT~~0(13)	~~TRIGBIT~~0(12)	GND	TRIGBIT7(12)	TRIGBIT7(11)	GND
7	GND	~~TRIGBIT~~0(15)	~~TRIGBIT~~0(14)	TRIGBIT7(15)	TRIGBIT7(14)	TRIGBIT7(13)	GND
8	GND	TRIGBIT1(2)	TRIGBIT1(1)	TRIGBIT1(0)	TRIGBIT6(1)	TRIGBIT6(0)	GND
9	GND	TRIGBIT1(4)	TRIGBIT1(3)	GND	TRIGBIT6(3)	TRIGBIT6(2)	GND
10	GND	TRIGBIT1(7)	TRIGBIT1(6)	TRIGBIT1(5)	TRIGBIT6(5)	TRIGBIT6(4)	GND
11	GND	TRIGBIT1(9)	TRIGBIT1(8)	GND	TRIGBIT6(7)	TRIGBIT6(6)	GND
12	GND	TRIGBIT1(11)	TRIGBIT1(10)	TRIGBIT6(10)	TRIGBIT6(9)	TRIGBIT6(8)	GND
13	GND	TRIGBIT1(13)	TRIGBIT1(12)	GND	TRIGBIT6(12)	TRIGBIT6(11)	GND
14	GND	TRIGBIT1(15)	TRIGBIT1(14)	TRIGBIT6(15)	TRIGBIT6(14)	TRIGBIT6(13)	GND
15	GND	TRIGBIT2(2)	TRIGBIT2(1)	TRIGBIT2(0)	TRIGBIT5(1)	TRIGBIT5(0)	GND
16	GND	TRIGBIT2(4)	TRIGBIT2(3)	GND	TRIGBIT5(3)	TRIGBIT5(2)	GND
17	GND	TRIGBIT2(7)	TRIGBIT2(6)	TRIGBIT2(5)	TRIGBIT5(5)	TRIGBIT5(4)	GND
18	GND	TRIGBIT2(9)	TRIGBIT2(8)	GND	TRIGBIT5(7)	TRIGBIT5(6)	GND
19	GND	TRIGBIT2(11)	TRIGBIT2(10)	TRIGBIT5(10)	TRIGBIT5(9)	TRIGBIT5(8)	GND
20	GND	TRIGBIT2(13)	TRIGBIT2(12)	GND	TRIGBIT5(12)	TRIGBIT5(11)	GND
21	GND	TRIGBIT2(15)	TRIGBIT2(14)	TRIGBIT5(15)	TRIGBIT5(14)	TRIGBIT5(13)	GND
22	GND	TRIGBIT3(2)	TRIGBIT3(1)	TRIGBIT3(0)	~~TRIGBIT~~4(1)	~~TRIGBIT~~4(0)	GND
23	GND	TRIGBIT3(4)	TRIGBIT3(3)	GND	~~TRIGBIT~~4(3)	~~TRIGBIT~~4(2)	GND
24	GND	TRIGBIT3(7)	TRIGBIT3(6)	TRIGBIT3(5)	~~TRIGBIT~~4(5)	~~TRIGBIT~~4(4)	GND
25	GND	TRIGBIT3(9)	TRIGBIT3(8)	GND	~~TRIGBIT~~4(7)	~~TRIGBIT~~4(6)	GND
26	GND	TRIGBIT3(11)	TRIGBIT3(10)	~~TRIGBIT~~4(10)	~~TRIGBIT~~4(9)	~~TRIGBIT~~4(8)	GND
27	GND	TRIGBIT3(13)	TRIGBIT3(12)	GND	~~TRIGBIT~~4(12)	~~TRIGBIT~~4(11)	GND
28	GND	TRIGBIT3(15)	TRIGBIT3(14)	~~TRIGBIT~~4(15)	~~TRIGBIT~~4(14)	~~TRIGBIT~~4(13)	GND
29	GND	GND	GND	GND	GND	GND	GND
30	GND	TRIGBIT3(17)	TRIGBIT3(16)	GND	~~TRIGBIT~~4(17)	~~TRIGBIT~~4(16)	GND
31	GND	TRIGBIT3(19)	TRIGBIT3(18)	GND	~~TRIGBIT~~4(19)	~~TRIGBIT~~4(18)	GND
32	GND	~~TRIGBIT~~3(21)	B0_DELAYED3	~~TRIGBIT~~4(22)	~~TRIGBIT~~4(21)	B0_~~DELAYED~~4	GND
33	GND	~~TRIGBIT~~3(23)	~~TRIGBIT~~3(22)	GND	TRIGBIT5(16)	~~TRIGBIT~~4(23)	GND
Connector Key (equivalent to 3 pins)							
34	GND	TRIGBIT2(17)	TRIGBIT2(16)	GND	TRIGBIT5(18)	TRIGBIT5(17)	GND
35	GND	TRIGBIT2(19)	TRIGBIT2(18)	GND	B0_DELAYED5	TRIGBIT5(19)	GND
36	GND	~~TRIGBIT~~2(22)	~~TRIGBIT~~2(21)	B0_DELAYED2	~~TRIGBIT~~5(22)	~~TRIGBIT~~5(21)	GND
37	GND	TRIGBIT1(16)	~~TRIGBIT~~2(23)	GND	TRIGBIT6(16)	~~TRIGBIT~~5(23)	GND
38	GND	TRIGBIT1(18)	TRIGBIT1(17)	GND	TRIGBIT6(18)	TRIGBIT6(17)	GND
39	GND	B0_DELAYED1	TRIGBIT1(19)	GND	B0_DELAYED6	TRIGBIT6(19)	GND
40	GND	~~TRIGBIT~~1(22)	~~TRIGBIT~~1(21)	~~TRIGBIT~~6(23)	~~TRIGBIT~~6(22)	~~TRIGBIT~~6(21)	GND
41	GND	~~TRIGBIT~~0(16)	~~TRIGBIT~~1(23)	GND	TRIGBIT7(17)	TRIGBIT7(16)	GND
42	GND	~~TRIGBIT~~0(18)	~~TRIGBIT~~0(17)	GND	TRIGBIT7(19)	TRIGBIT7(18)	GND
43	GND	B0_DELAYED0	~~TRIGBIT~~0(19)	GND	~~TRIGBIT~~7(21)	B0_DELAYED7	GND
44	GND	~~TRIGBIT~~0(23)	~~TRIGBIT~~0(22)	~~TRIGBIT~~0(21)	~~TRIGBIT~~7(23)	~~TRIGBIT~~7(22)	GND

Figure 1: Schematic of half of J3 backplane for Level 1 calorimetry crate.

Table 5: Pin assignments for Auxiliary board Input connectors J1-J12

Pin	Signal	Pin	Signal
1	BIT0	2	$\overline{\text{BIT0}}$
3	BIT1	4	$\overline{\text{BIT1}}$
5	BIT2	6	$\overline{\text{BIT2}}$
7	BIT3	8	$\overline{\text{BIT3}}$
9	BIT4	10	$\overline{\text{BIT4}}$
11	BIT5	12	$\overline{\text{BIT5}}$
13	BIT6	14	$\overline{\text{BIT6}}$
15	BIT7	16	$\overline{\text{BIT7}}$
17	BIT8	18	$\overline{\text{BIT8}}$
19	BIT9	20	$\overline{\text{BIT9}}$