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Specification for Trigger Tower Summing and E_T Weighting for ADMEM Boards

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1 Introduction

The ADC/Memory (ADMEM) boards digitize the calorimeter phototube signals and store the digitized data during the L1 and L2 trigger processing. In addition the ADMEM forms the trigger tower transverse energies. Single tube data is summed over one to four phototubes[1] to form trigger towers and weighted by $\sin\theta$. The resulting 10 bit words are transmitted over parallel copper cables to the DIRAC boards of the L1 calorimeter trigger. More details are available in the hardware specification of the ADMEM board[2].

A previous note[1] described the segmentation of the trigger towers, which phototubes are included in each tower, and the E_T weighting of each tower. Here we describe the algorithm required to form calorimeter trigger tower energy sums on the ADMEM board.

2 Algorithm for Trigger Summing and E_T Weighting

The trigger summing is carried out in the ADMEM digital pipeline chips each of which handles 4 input channels (implemented in XILINX FPGAs). The E_T weighting is then carried out in Flash Random Access Memory (FRAM).

2.1 Summing

Input: 1, 2 or 4 digitized pulse-heights, linearized and gain corrected. 16 bit output of linearization FRAMs on CAFE card, bit 15 is range bit (x8). A pedestal is added by the linearization FRAM.
Output: 15 bits of pedestal subtracted, summed trigger tower energy. Energy/count is optimized by summing region for best use of dynamic range.

4 Tube Sum (Central, Wall, and Plug)

1. Subtract pedestal from each tower (assumed to be single value for all channels, either range).

2. Convert each tower to single range, output 18 bits/channel
3. Sum 4 channels, output of 20 bits
4. Truncate to 15 bits, by dropping 2 least significant bits and 3 most significant bits.
5. If any of higher truncated bits (20:17) are on, then turn on all 15 output bits (saturate output in case of overflow). The three most significant bits are OR'd together and the result OR'd with the 15 output bits.

2 Tube Sum (Plug)

1. Subtract pedestal from each tower (assumed to be single value for all channels, either range).
2. Convert each tower to single range, output 18 bits/channel
3. Sum 2 channels, output of 19 bits
4. Truncate to 15 bits, by dropping 4 least significant bits

1 Tube "Sum" (Plug)

1. Subtract pedestal from tower (assumed to be single value for all channels, either range).
2. Convert to single range, output 18 bits/channel
3. Truncate to 15 bits, by dropping 3 least significant bits

2.2 Weighting

The summed outputs from the pipeline chips are passed to Flash RAMs which provide the E_T weighting. In addition, these will convert from the nominal MeV/count of the linearization FRAM to a standard 125 MeV/count. If the pedestal subtraction cannot be carried out in the pipeline chip it may be carried out here although limitations on the pedestal values will be required (see below).

Input: 15 bits of pedestal subtracted, summed trigger tower energy

Output: 10 bits of trigger tower transverse energy E_T, 125 MeV/count

Algorithm:
1. Form energy: $E = SCL_d * 2^n *$INPUT
2. Weight: $\mathrm{E}_T = E * \sin\theta_{tr}$
3. Integerize: OUTPUT = INT(E_T/125. + 0.5)
4. Truncate: If (OUTPUT>1023) OUTPUT=1023

Where:

SCL_d nominal number of MeV/count out of the linearization FRAM for the particular detector region (d=CEM,CHA,WHA,PEM,PHA)

n is the number of lsb dropped in the summing stage

$\sin\theta_{tr}$ is the weight for this trigger tower

Table 1: Energy scale factors for different detector regions after linearization in CAFE card FRAM.

Detector Region	Scale (SCL) (MeV/Count)
CEM	3
CHA	3
WHA	3
PEM	4
PHA	5

3 Choosing lsb of the Summer Output

The dynamic range of the summer output is set at 15 bits by the PC board design and chip choices. However, by carefully choosing the least significant bit out of the summer we can optimize the use of that dynamic range. The lsb will vary depending on trigger tower because of the wide range of weights in the E_T weighting FRAM (0.1-1.0) and because the different detector systems will have different energy scale factors (SCL) which describe the number of MeV/count. Vaia Papadimitrou has studied the maximum charge (energy) deposition expected for each detector in Run II[3]. The planned scale factors (SCL)[4] are listed in Table 1. The SCL gives the energy per count for the input to the summer.

We optimize the input to the trigger weighting FRAM by minimizing the quantization error while ensuring that the full scale does saturate. The former constraint is satisfied by minimizing the number of low order bits dropped. The latter constraint requires that:

$$FullScaleInput \times SCL_d \times \sin\theta_{tr} > 127.675\text{GeV}$$

or

$$FullScaleInput > \frac{127.675\text{GeV}}{SCL * \sin\theta_{tr}}.$$

If the full scale of the input were smaller then we could never reach 128 GeV in a trigger tower. Table 2 lists the trigger tower summing and weighting for Central, Wall and Plug ADMEM boards. Listed are the trigger output channel, summed input channels, $\sin\theta_{tr}$ for the tower, and the energy corresponding to full scale E_T output. The 5th and 7th coulumns of the table give the minimum requirement for the full scale input to the weighting FRAM for the hadron and EM respectively. The adjacent columns give the corresponding most significant bit required to cover this full scale.

For simplicity we choose one granularity for each summing type: single tower, two towers, and 4 towers independent of detector region. In the four channel sums, where there are 20 bits out of the summing stage, we will drop the 2 LSB and the 3 MSB. This will result in a maximum quantization error of 12 MeV for Central, 9 MeV Wall, 9 MeV for PEM and 7 MeV for PHA. In the single channel towers, which have 18 bits we simply drop the 3 LSB. The maximum quantization error is

7 MeV for PEM and 9 MeV for PHA. For the two channel sum, with 19 bits, we drop the lowest 4 bits resulting in a quantization error of 6 MeV for PEM and 8 MeV for PHA.

References

[1] H.J Frisch, M. Shochet, G. Sullivan, P.J. Wilson, *Trigger Tower Organization and Summing in $\eta - \phi$ space for Run II and Beyond*, CDF/DOC/TRIGGER/CDFR/2045, 1995.

[2] T. Shaw, *Specification for ADC/Memory Module (ADMEM)*, CDF/DOC/CALORIMETRY/PUBLIC/4685, 1997.

[3] P. Chang and V.Papadimitriou, *Specifications for Calorimeter Front-End Electronics*, CDF/DOC/CALORIMETRY/CDFR/3646, 1996.

[4] Mike Lindgren, *What's a Calorimeter ADC Count*, DAQ Meeting, 1/7/98.

Table 2: Trigger tower summing and weighting for ADMEM boards. The input and output channels involved for each trigger tower are listed. The full scale energy, 128 GeV/$\sin\theta$ ($E = \mathrm{E}_T/\sin\theta$), for each trigger tower is given in the 5th column. The equivalent full scale counts out the summing (columns 6 and 8 for HAD and EM respectively) is given by dividing couln 5 by the scale (SCL_d). Mimimal required most significant bit is given in columns 7 and 9.Three types of ADMEM boards are covered: Central, Wall and Plug. The EM and Hadron boards are identical.

Trigger Tower	ADMEM Output	ADMEM Inputs	$\sin\theta$ Tower	$\frac{128\text{ GeV}}{\sin\theta}$	Hadron FS Counts	Hadron FS MSB	EM FS Counts	EM FS MSB
Central:								
0	0	0-3	0.992	129	43K	16	43K	16
1	1	4-7	0.932	137	46K	16	46K	16
2	2	8-11	0.839	152	51K	16	51K	16
3	3	12-15	0.740	173	58K	16	58K	16
4	4	16-19	0.646	198	-	-	66K	17
Wall:								
3	0	0-3	0.740	173	58K	16	-	-
4	1	4-7	0.646	198	66K	17	-	-
5	2	8-11	0.551	232	73K	17	-	-
Plug:								
5	0	0-3	0.551	232	-	-	58K	16
6	1	4-7	0.459	279	56K	16	70K	17
7	2	8-11	0.373	343	69K	17	86K	17
8	3	12-15	0.284	450	90K	17	112K	17
9	4	16	0.216	593	119K	17	148K	18
10	5	17	0.169	757	151K	18	198K	18
11	6	18-19	0.103	1243	249K	18	311K	19