ADC Architecture

Sampling channel: 4
ADC: 125/Channel
Ramp Gen.: 1
Super Buffer/Driver: 4
Schematic Diagram of Ramp Generator and Super Buffer/Driver
Schematic of Super Buffer/Driver
Simulation of Super Buffer/Driver

- Capable to drive 125 comparators (huge load)
- Gian-1 Stable
- Adequate bandwidth (slew rate and noise etc)
- Linearity and dynamic range

Compensation Cap = 1pf with 2pf load

Compensation Cap = 2pf with 2pf load
Simulation Results of Ramp Gen. & Super Buffer/Driver

Non Linearity = ~20%, It can be calibrated off-line
Summary

- Simple current source and low rail voltage presents big non-linearity on ramping current.
- Non-linearity can be calibrated off-line.

Work need to be done:

- Layout
- Post layout simulation
- Minor tuning on gate parameters may be required after post layout simulation
Thank you for your review