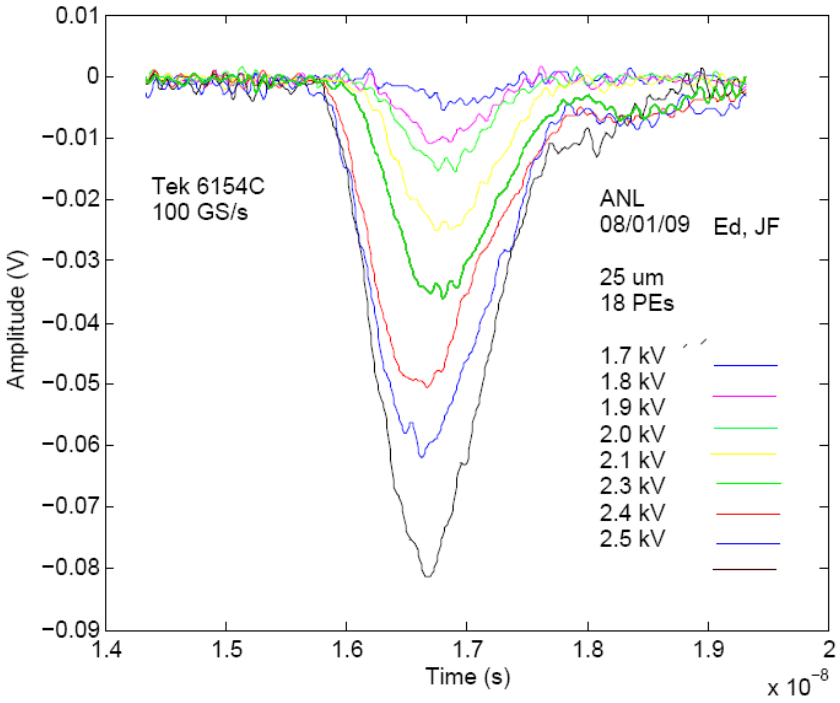
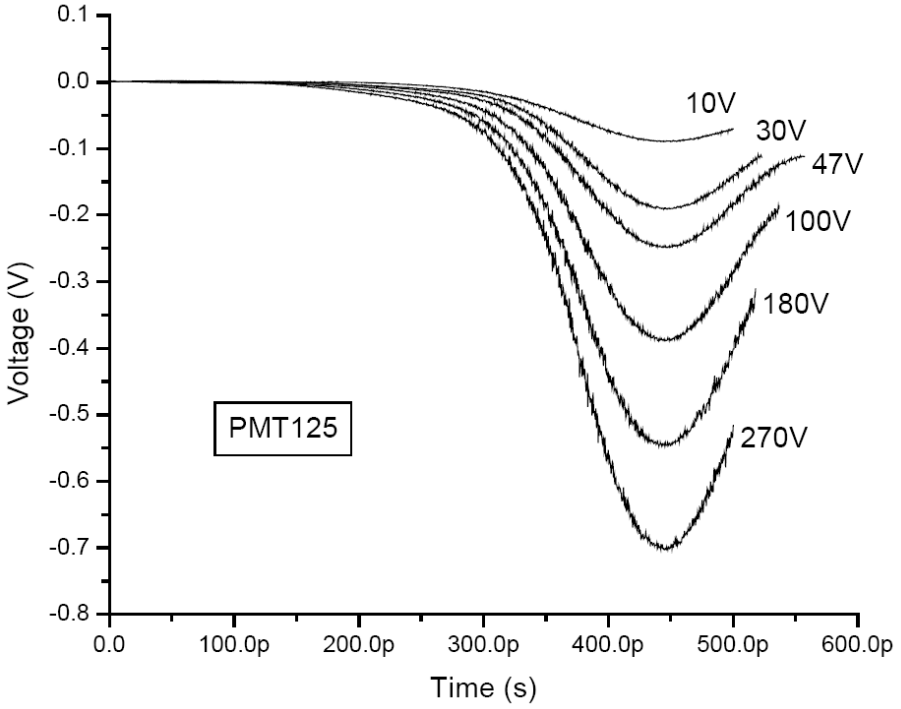
Microchannel Plates signals, Picosecond timing, Design’s minimum performance

MCP signals

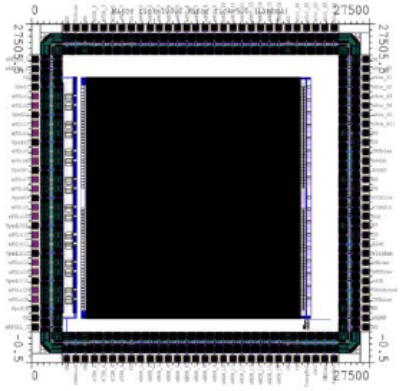
- left: 1024 pads 25 μm MCP recorded at Argonne.
  Bandwidth is 1 GHz
- right: MCP from Photek 6 μm MCP
  Bandwidth is 3 GHz

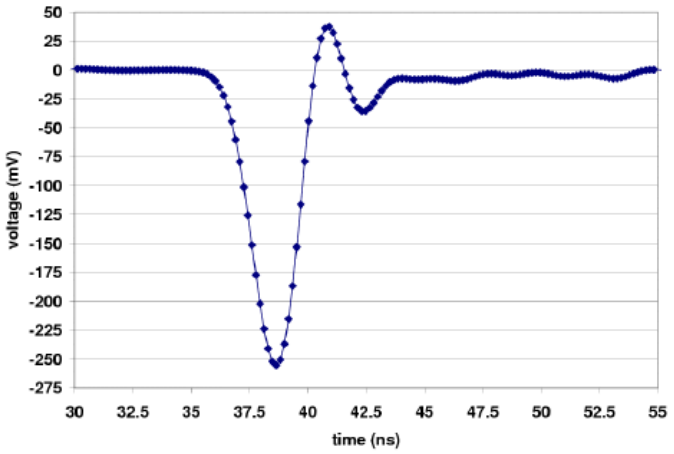




Picosecond timing

Fast sampling allows reconstructing the time of arrival to a few picoseconds knowing the waveform.





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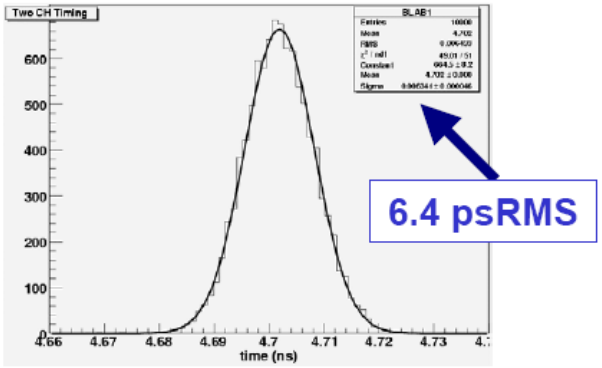
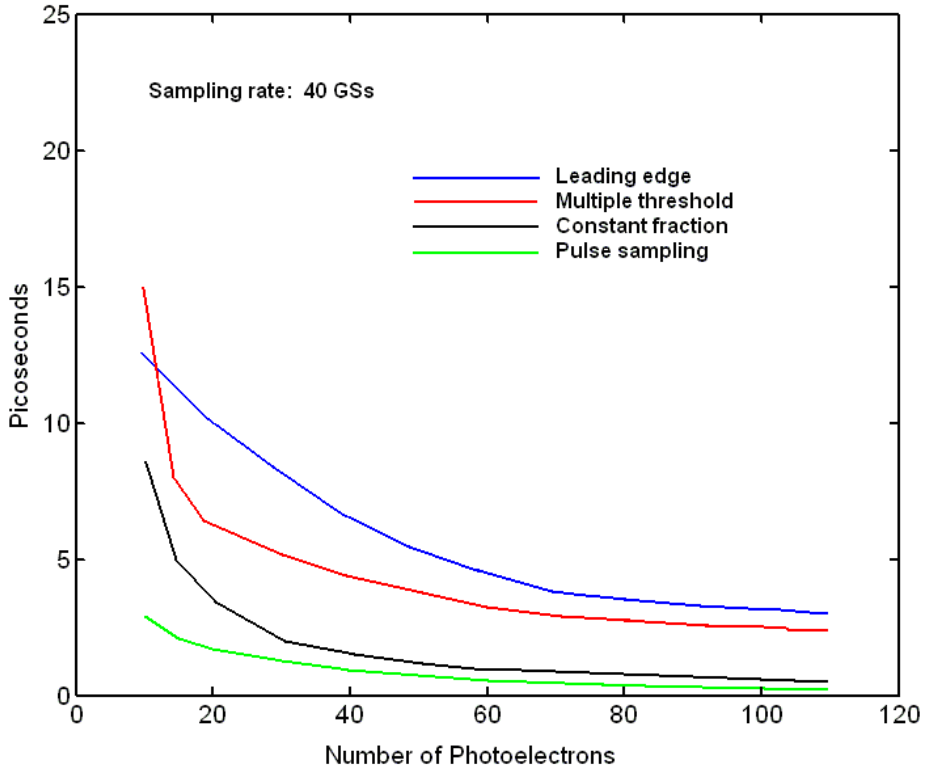
ps Timing Workshop, March 2008

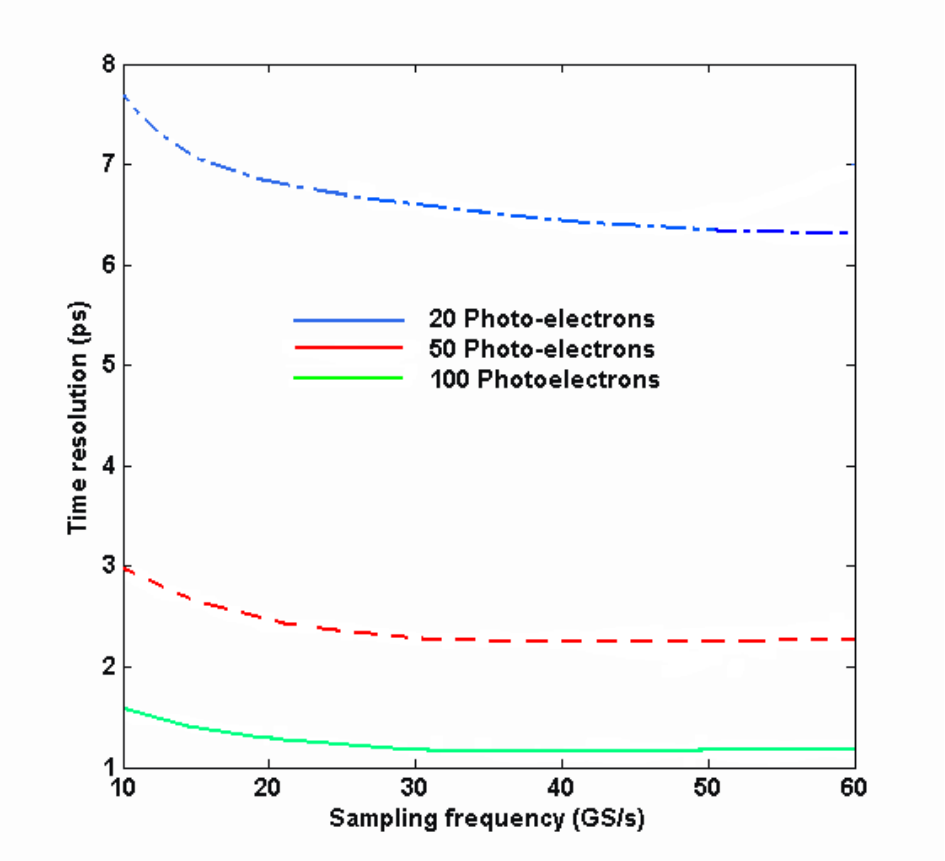


Timing using fast sampling



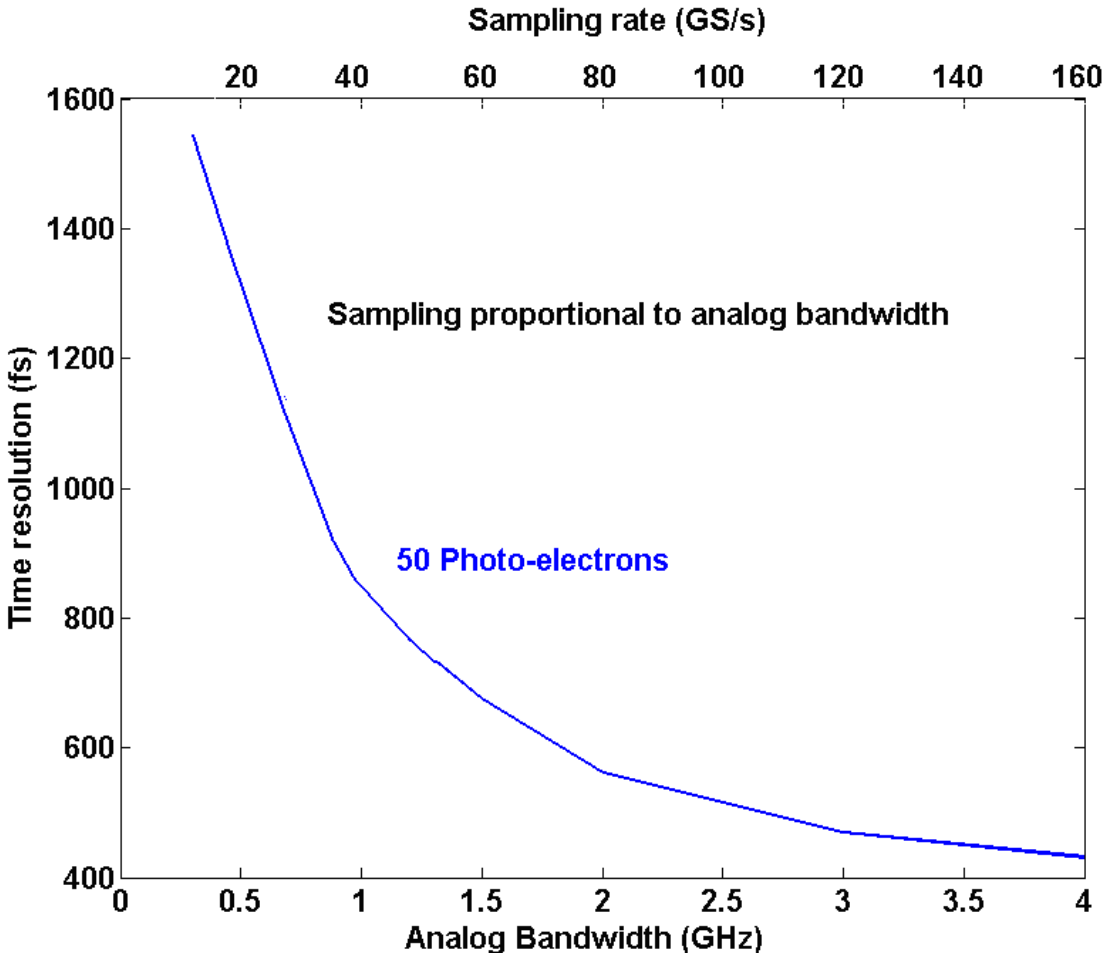
Simulated timing resolution using fast sampling
S/N=80 at 50PEs (white + detector noises)

Sampling rate and analog bandwidth



Simulated timing resolution vs Sampling rate
50PEs (white + detector noises)

Sampling rate and analog bandwidth



Simulated timing resolution vs Sampling rate and analog bandwidth
50PEs (white + detector noises)

Design's minimum performance

	Hawaii		/Orsay/Saclay		PSI		PSEC
	Lab 3	**Planned Blab2**	**Sam**	**Planned**	**DRS3**	**Planned DRS4**	**This proposal**
Sampling frequency	20 MHz-3.7 GHz	1-10 GHz	0.7-2.5 GHz	10 GHz	10 MHz-5 GHz	5 GHz	40 GHz
Analog bandwidth	900 MHz	850 MHz	300 MHz	650 MHz	450 MHz	> DRS3	>1 GHz
Number of Channels	9	16	2		12/6/2/1	8/4/2/1	16
Triggered mode	Common Stop	Channel trigger on sums	Common Stop		Common Stop	Common Stop	Channel trigger
Resolution		10 bit	11.6 bit		11.6 bit	11.5 bit	8-10 bit
Samples	256	4/8 rows of 512	256	2048	1024-12288	1024-8192	64
Clock	33 MHz	33 MHz	66 MHz		20 MHz	fsamp/2048	60 MHz
Max latency			5ms		0.6 ms		
Input Buffers		TIA (5kOhm gain)	Yes	No	No	No	Yes
Differential inputs	No	Pseudo-diff	Yes		Yes	Yes	Pseudo diff
Input impedance	50 Ohms Ext	30-70Ohms adjustable	> 10 MOhm			7-11pF	
Readout clock		1 GHz Wilkinson	16 MHz		33 MHz	33 MHz	60 MHz
Readout time	150µs	512µs	< 2 µs		30ns * n_samples	30ns * n_samples	< 1 µs
Locked delays	Ext DAC	Ext DLL	Int DLL		Ext PLL	Int PLL	
On-chip ADC	Yes	1 GHz Wilkinson	No		No	No	Yes
R/W simultaneous		Yes	No		No	Yes	No
Power/ch	50mW	20mW/sample 0.2W/read	150 mW		1-13mW	2-20mW	
Dynamic range		1mV/1V	0.65mV-2V		0.35mV/1.1V	0.35/1V	1V
Xtalk	Average <<10%	< 0.1%	0.30%		<0.5%	<0.5%	
Sampling jitter		TBD	40ps		200ps (Ext PLL)	Ext PLL	10ps
Power supplies	2.5V	2.5V	0-3.3V		2.5V	2.5 V	1.8V
Process	TSMC 0.25	TSMC 0.25	AMS 0.35	AMS 0.18	UMC 0.25	UMC 0.25	CMOS 0.13
Chip area	2.5 mm2	12 mm2	10 mm2		25 mm2	25 mm2	1 mm2
Cost/channel		500$/40 10$/2k	15.7$/12k			10-15$	