General Idea

<table>
<thead>
<tr>
<th>Clock Cycle</th>
<th>Token Start</th>
<th>Bit Switch Active</th>
</tr>
</thead>
<tbody>
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</tr>
<tr>
<td>2</td>
<td>0</td>
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</tr>
<tr>
<td>3</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
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<td>:</td>
</tr>
<tr>
<td>130</td>
<td>0</td>
<td>128</td>
</tr>
</tbody>
</table>

ADC

Register #1

Register #2

Register #128

Token Control

Bit #1 SB

Bit #2 SB

Bit #12 SB

Token Start

Clock

12
Bit Switch Box

Stage 1 (16) → Stage 2 (8)
Bit Switch Box

~400ps Delay (no load)
Token Control
Token Control
Token Control

~200ps Delay (no load)
Full Readout Schematic

Register (Emilien)

Token Control

Bit Switch Boxes

12 bit Output Bus

x 128