Storage cell – Psec timing project

- Herve Grabas -

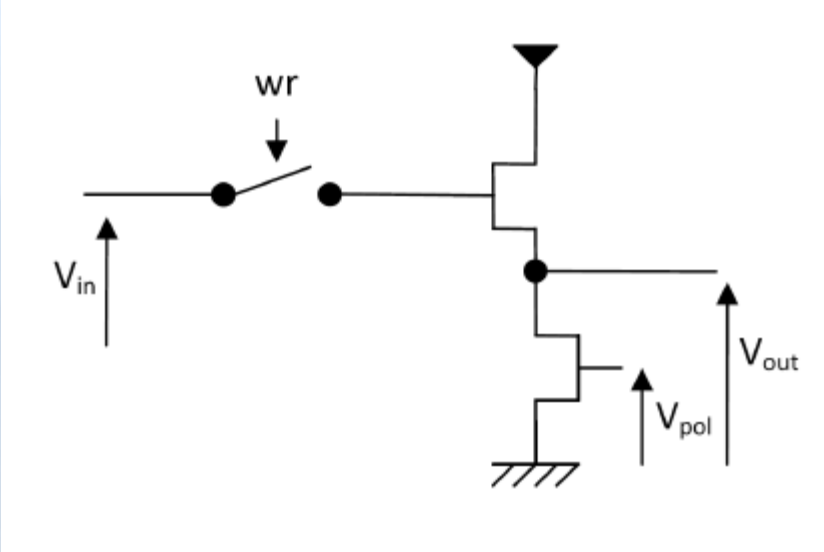
Cell principle

We use a source follower structure.

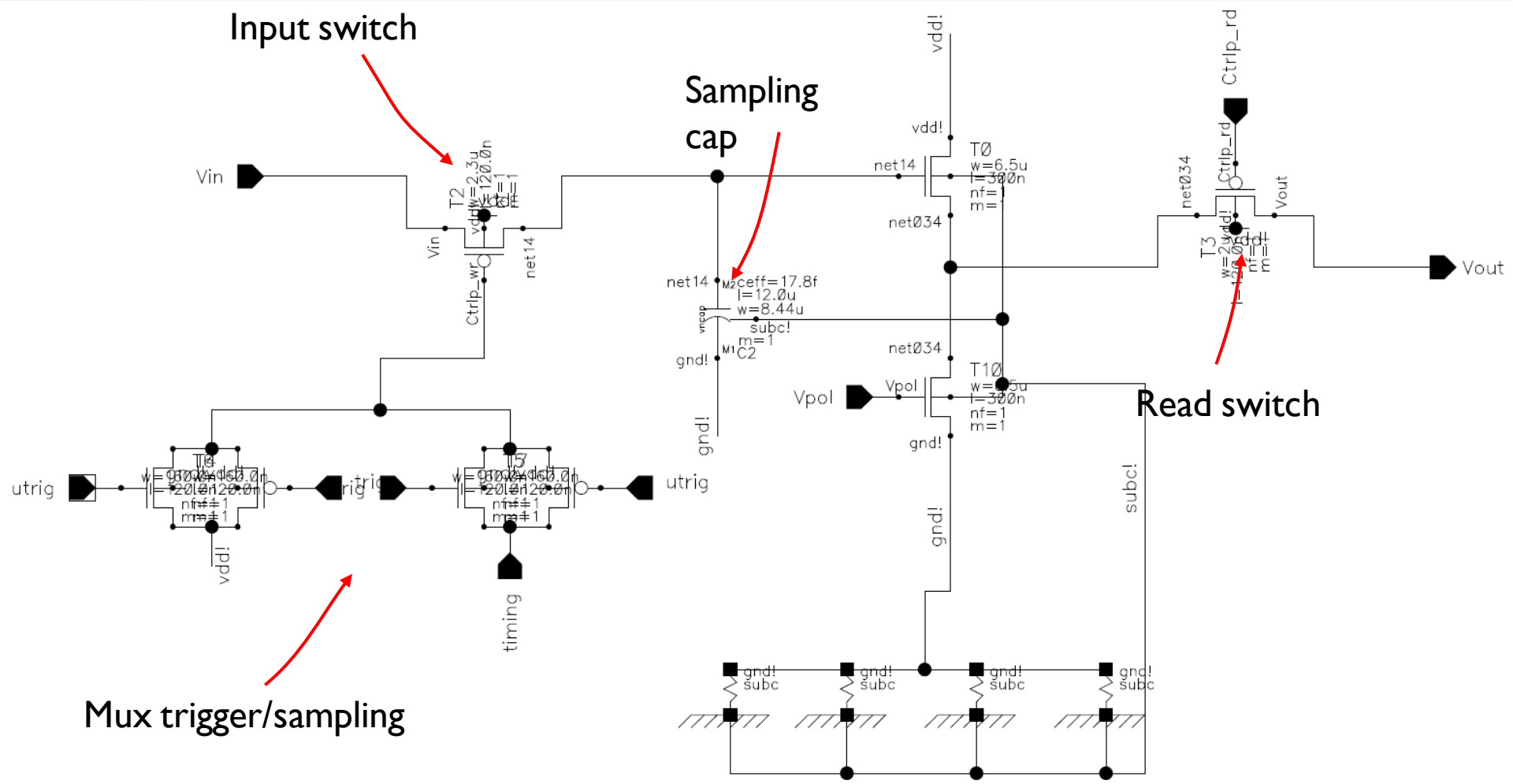
The polarization tension Vpol gives the drop of tension between Vin and Vout.

An additional capacitance is added at the entrance of the Nfet for noise limitation (kT/C).

Characteristics :
Nfet : 300nm x 6.5µm
Capacitance : 20 fF
Vpol = 400mV



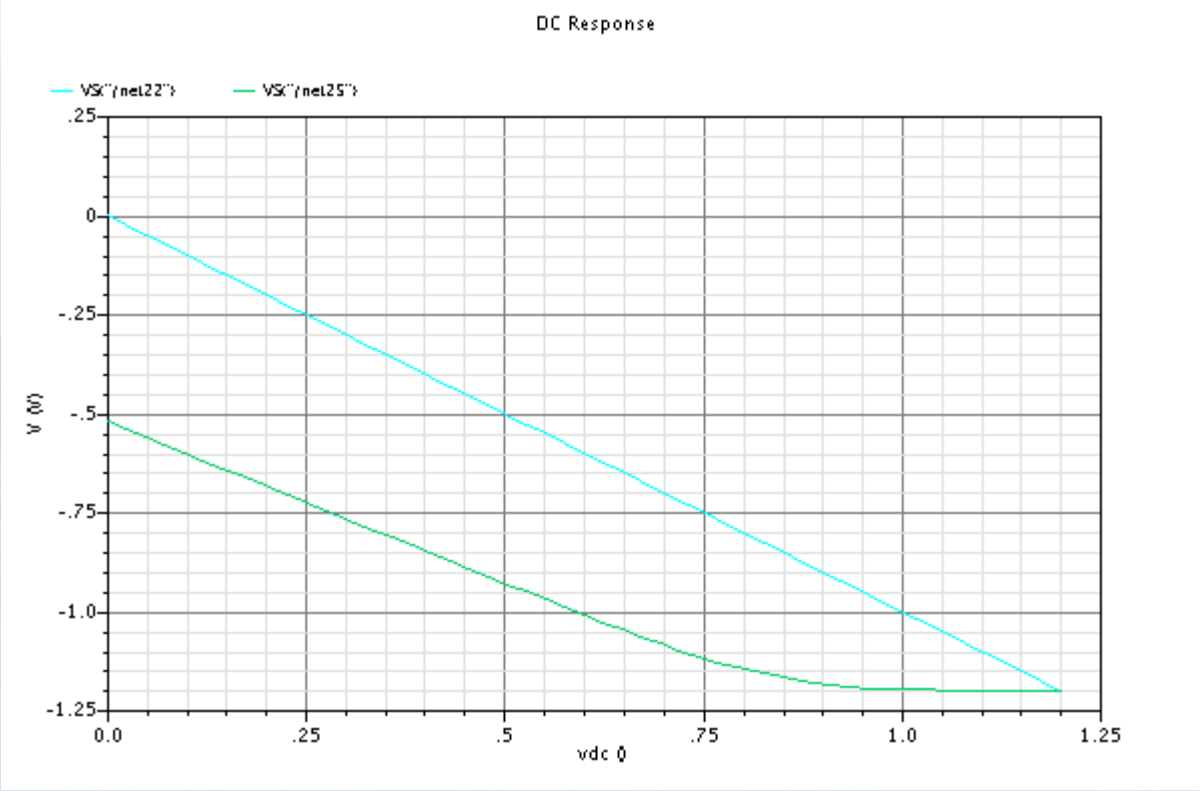
$$V_{out} = Vin - V_T - (V_{pol} - V_T)\sqrt{\frac{W}{L}\frac{L_{pol}}{W_{pol}}}$$


Input switch
Sampling cap
Read switch
Mux trigger/sampling
Vin
Vout
Vpol
utrig
timing
vdd!
gnd!
subc!
net14
net034
Ctrlp_rd
Ctrlp_wr
T2
T0
T10
T3
T4
T5
C2
M2
ceff=17.8f
l=12.0u
w=8.44u
m=1
nf=1
gnd!
subc

Results : DC Charac

Big drop of tension due to the source follower: 500mV
The output dynamic is consequently reduced

Output dynamic: 700mV

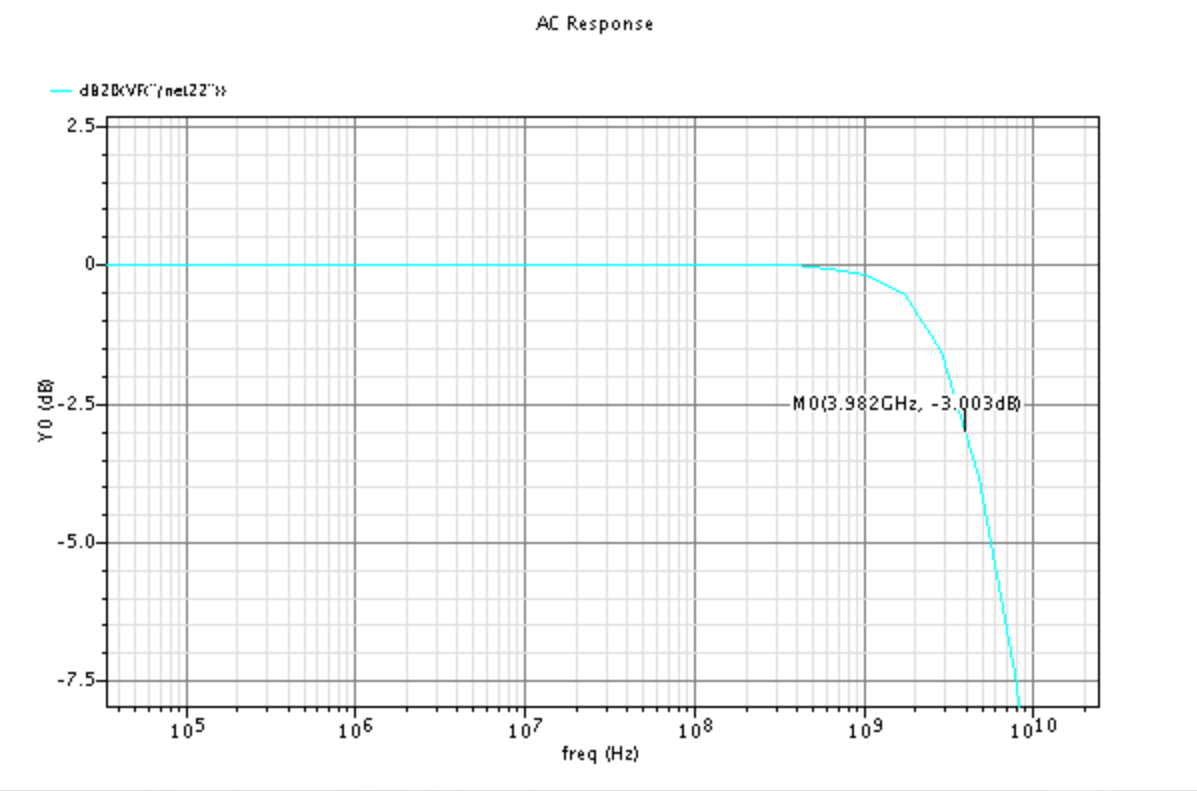


Results: Bandwidth

Cutoff frequency: 4GHz (prelayout)
Ron = 1.2kΩ
Cin = 15fF + 17fF

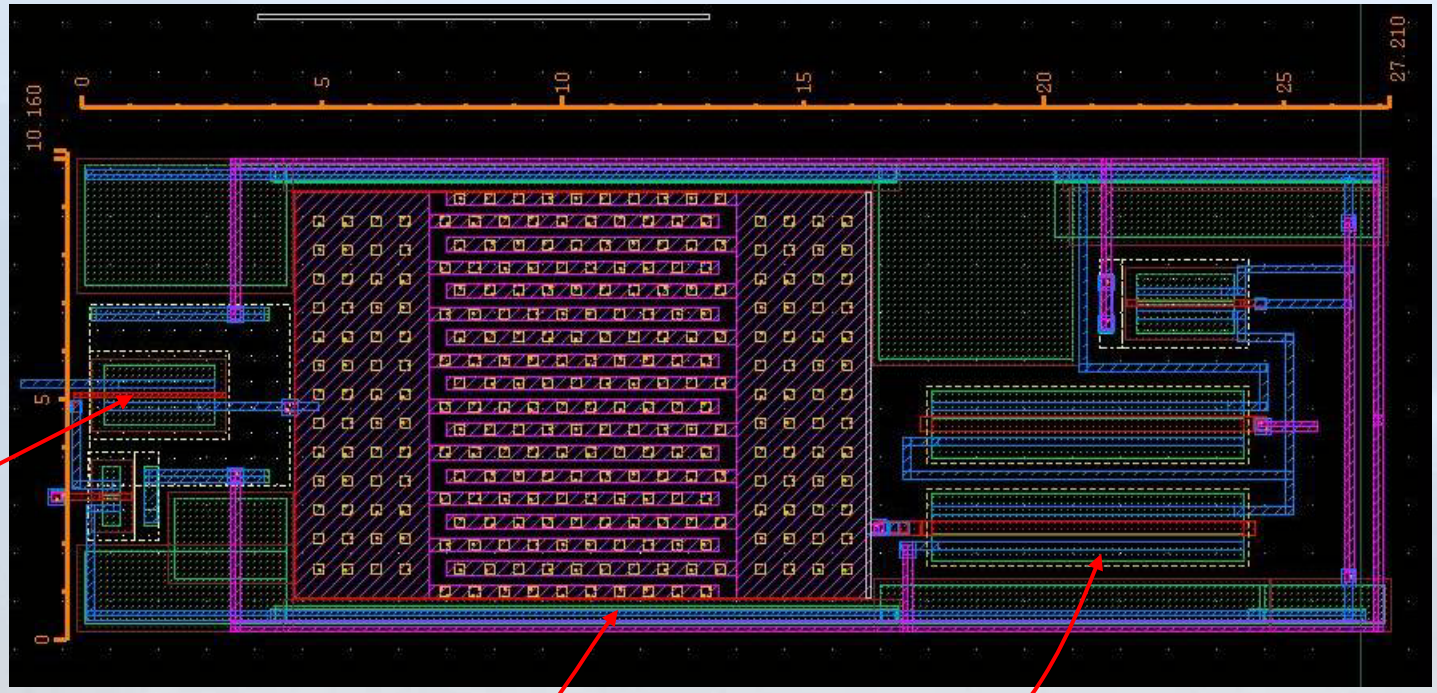
This is only for one cell. Have to be checked for 125 cells.

If bandwidth issue Ron can be reduced a bit more. But then beware of leakage current at the input.



Layout dimensions

Previous layout: dimension should remain the same



Bandwidth

- Input bandwidth and signal:

Actually we put the input signal on 64 cells witch means :

- f_3dB = 1/2.pi.Z.Ctot

  Z= 50 Ohms

  Ctot = 125*Cd (off) + 64*Csto

  Cd = 500aF & Csto = 40fF

- Cd appears to be small enough

Input lines

- Layout of the input lines
- To reduced reflexion we want a 50 Ohms impedance for the line.
- 50 Ohm matching is possible using 2 layers of metal with a given width.

Leakage current

- Leakage current
- Target: 4μs window for digitization.
- Due to the process used the leakage current at the input is relatively high.
- Using a Rd switched allow us to have an output stable even with a leaking input.