Foundry technologies 130-nm CMOS and RF CMOS

Highlights	
 Standard Features Twin-well CMOS technology on nonepitaxial p- doped substrate Low-resistance cobalt-silicide n+ and p+ doped polysilicon and diffusion regions Up to three thick copper wiring levels Four to eight levels of global copper metal (CMOS 8SFG) Five to eight levels of copper metal with an Al-Cu-Al last metal sequence (CMOS 8RF) Wire-bond or C4 solder-bump terminals 	

IBM 130-nm Technology Highlights

Category	Base Technology CMOS 8SFG	Related Technology CMOS 8RF	
Process	Industry-standard 130-nm CMOS	CMOS 8SFG additional passive devices	
Wiring	Copper	Copper and aluminum with analog metal	

Related technology

provide design flexibility.

IBM **CMOS 8RF** offers several enhancements to CMOS 8SFG including FET structures that support high-frequency RF-compatible models, a broad range of optional passive devices and copper and aluminum wiring with a thick last metal. A high-quality analog design

processing applications. CMOS 8SFG uses low-resistance copper wiring at all metal levels, enabling high wiring density with minimal timing delays. Up to three thick copper wiring metal options

kit ensures close correlation between simulated and measured performance. In addition, the technology maintains compatible design rules with the corresponding levels in CMOS 8SFG.

CMOS 8RF is an ideal semiconductor technology for low-cost, high-performance wireless applications such as Bluetooth[™] technologies, local area networks, handsets and global positioning systems.

For more information

For more information, contact IBM at foundry@us.ibm.com

CMOS Specifications (common to 130-nm technology family)

Lithography	130 nm	
Voltage (V _{DD})	1.2 V or 1.5 V	
Additional power supply options	2.5 V / 3.3 V I/O	
Standard NFET / PFET		
L _{min}	0.24 µm	
Lp	0.22 μm	
Vt	0.355 V / -0.30 V	
Dsat	530 mA / 210 mA	
I _{off}	300 pA/um / 250 pA/µm	
T _{ox}	2.2 nm	
Thick-oxide NFET / PFET		
L _{min}	0.24 µm	
Lp	0.22 μm	
Vt	0.41 V / -0.44 V	
I _{Dsat}	660 mA / 260 mA	
l _{off}	10 pA/µm / 10 pA/µm	
T _{ox}	5.2 nm	

Note: Specifications given for 1.2 V (nominal) at 25°C.

CMOS Specifications	CMOS 8SFG	CMOS 8RF
Isolation	Shallow trench	Shallow trench
Levels of metal	4–8	5–8
Metallization	Copper	Copper, Aluminum
FET devices (max. voltage)* Ultra-thin NFET / PFET (1.2V) Standard NFET / PFET (1.5V) Zero-Vt NFET (1.5V) Isolated NFET (1.5V) Low- Vt NFET / PFET (1.5V) High-Vt NFET / PFET (1.5V) Low-power NFET / PFET (1.5V) Thick-oxide NFET / PFET (2.5V) Thick-oxide Zero Vt NFET (2.5V) Thick-oxide Isolated NFET (2.5V))	-

*FET devices can be used in a variety of design options that are defined in the respective technology design manuals.



Passive Devices	CMOS 8SFG	CMOS 8RF
Capacitors		
MIM	1.35 fF/µm² ± 15%	1.35 fF/µm ² ± 15%
Single MIM	<u> </u>	2.0 fF/µm ² ± 10%
Dual MIM	_	4.1 fF/µm ² ± 10%
Thick-oxide MOS	5.85 fF/µm ² ± 10%	5.85 fF/μm ² ± 10%
Thin-oxide MOS	11.1 fF/μm² ± 10%	11.1 fF/µm² ± 10%
Fuses	Laser, e-fuse	e-fuse
Inductors*		
Analog metal spiral	_	Q = 10
Stacked dual-metal spiral	-	Q = 24
Resistors		
n+ diffusion	73 Ω/❑ ± 11%	73 Ω/❑ ± 15%
p+ polysilicon	340 Ω/❑ ± 12%	340 Ω/🛛 ± 20%
p- polysilicon	_	1450 Ω/❑ ± 25%
Tantalum nitride	-	60 Ω/❑ ± 6%
Varactors		
Hyperabrupt junction	_	\checkmark
MÓS	1	\checkmark

* All inductor measurements were taken at L = 1 nH and f = 2 GHz.

Design Tools	CMOS 8SFG	CMOS 8RF		
Models				
BSIM3	1	\checkmark		
Cadence Spectre	1	_		
Cadence SpectreRF	-	\checkmark		
IBM digital	1	_		
Synopsys HSPICE	1	1		
Verification tools				
Avant! Hercules	1	\checkmark		
Cadence Assura	_	\checkmark		
Mentor Graphics Calibre	1	1		
Libraries				
Artisan	1	\checkmark		
IBM	\checkmark	-		

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