Design Review

PSEC3 8-2-2010

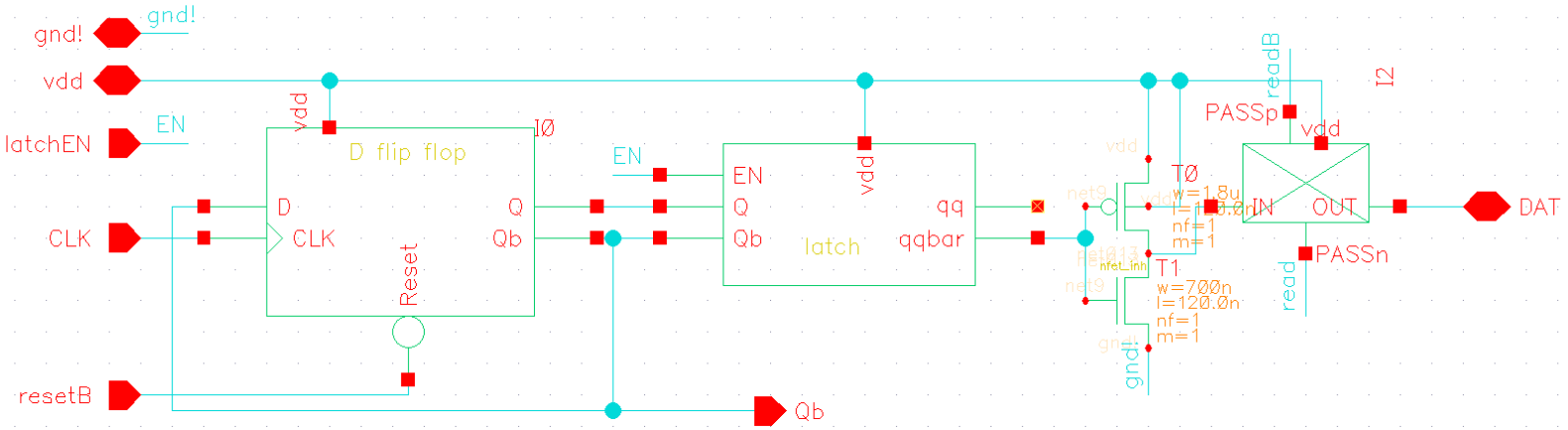
ADC

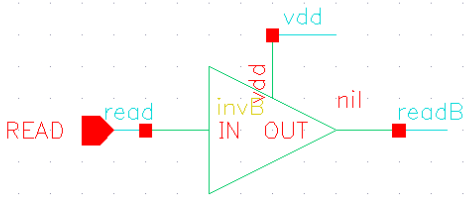
- digital structure
- specifications
- test points

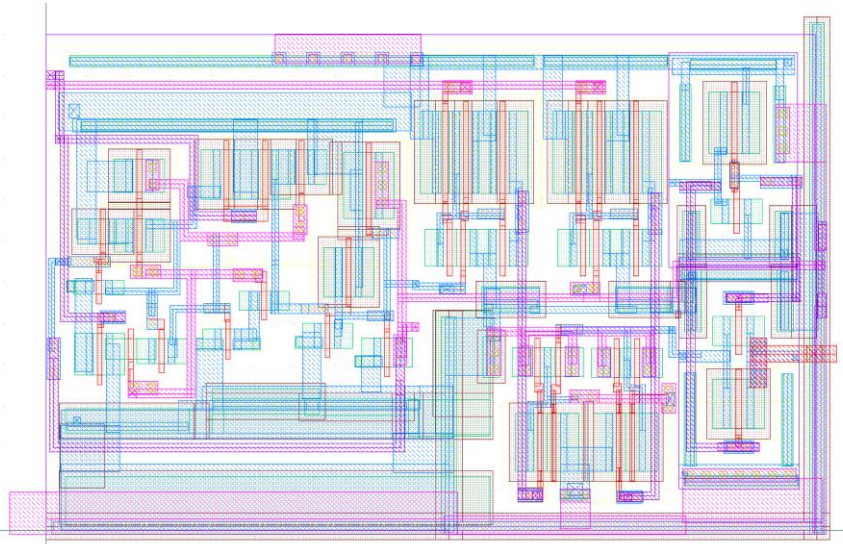
Eric Oberla

ADC

Up to 12 bit Wilkinson ADC with 2 stage structure of counter+storage (fast dff+latch)

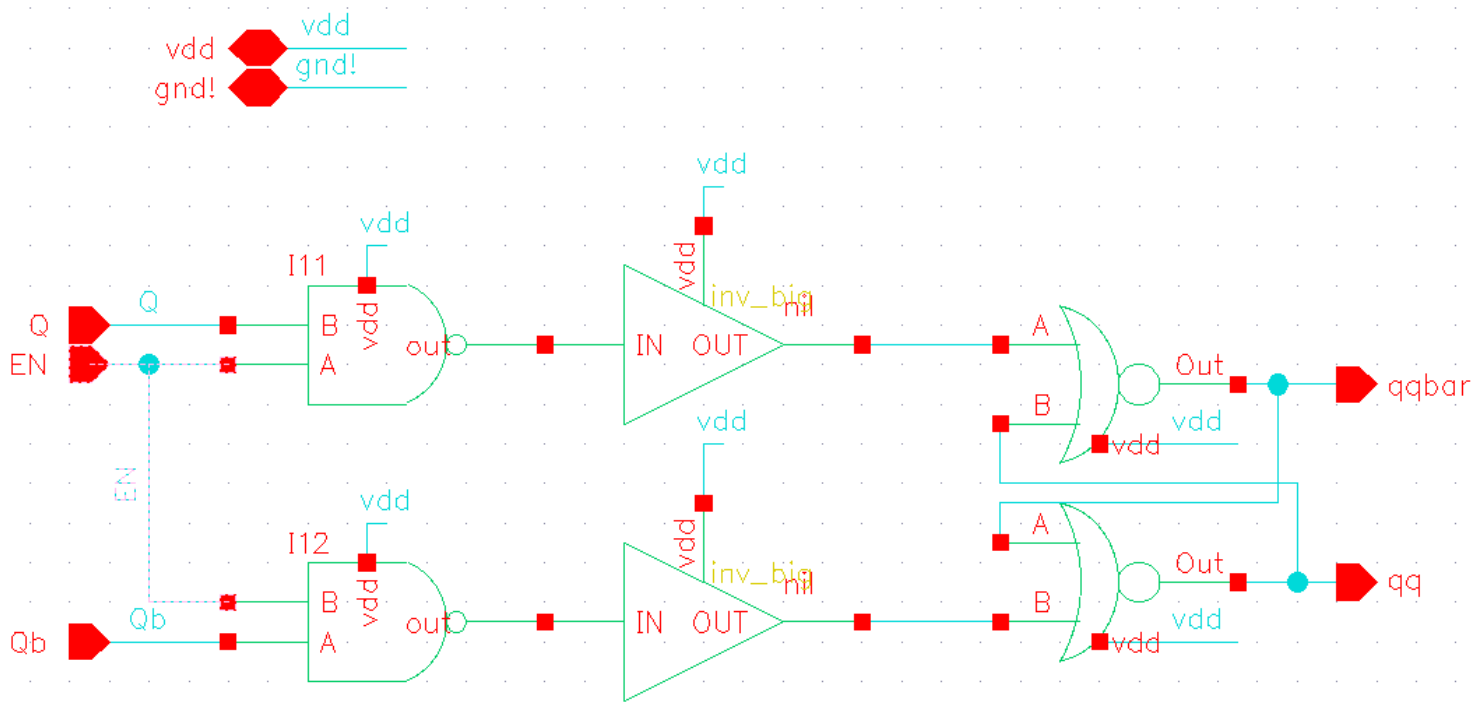






In the future, this 2-stage structure could be tweaked to allow concurrent readout and digitization (would drastically reduce dead-time).

ADC - latch



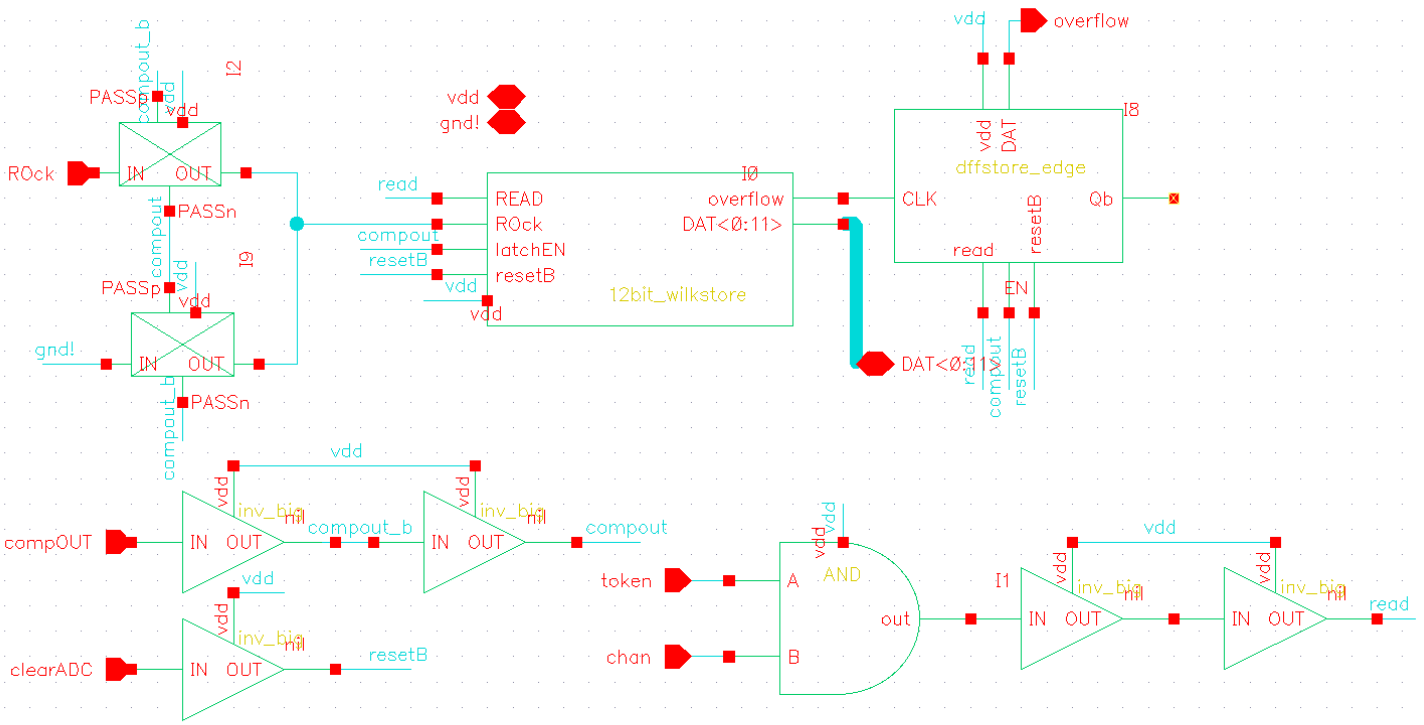
- Standard NOR latch with Enable input follows fast d flip flop.

  EN = 1 : latch is transparent

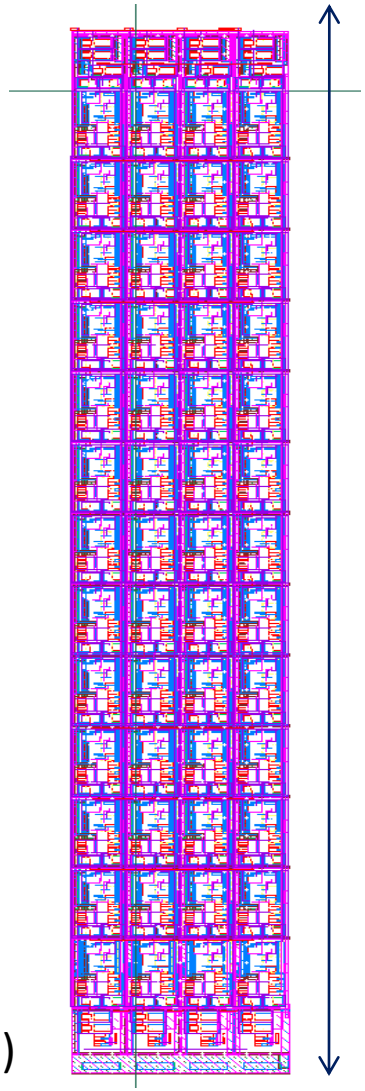
  EN = 0 : latch stores last value

ADC

One cell:



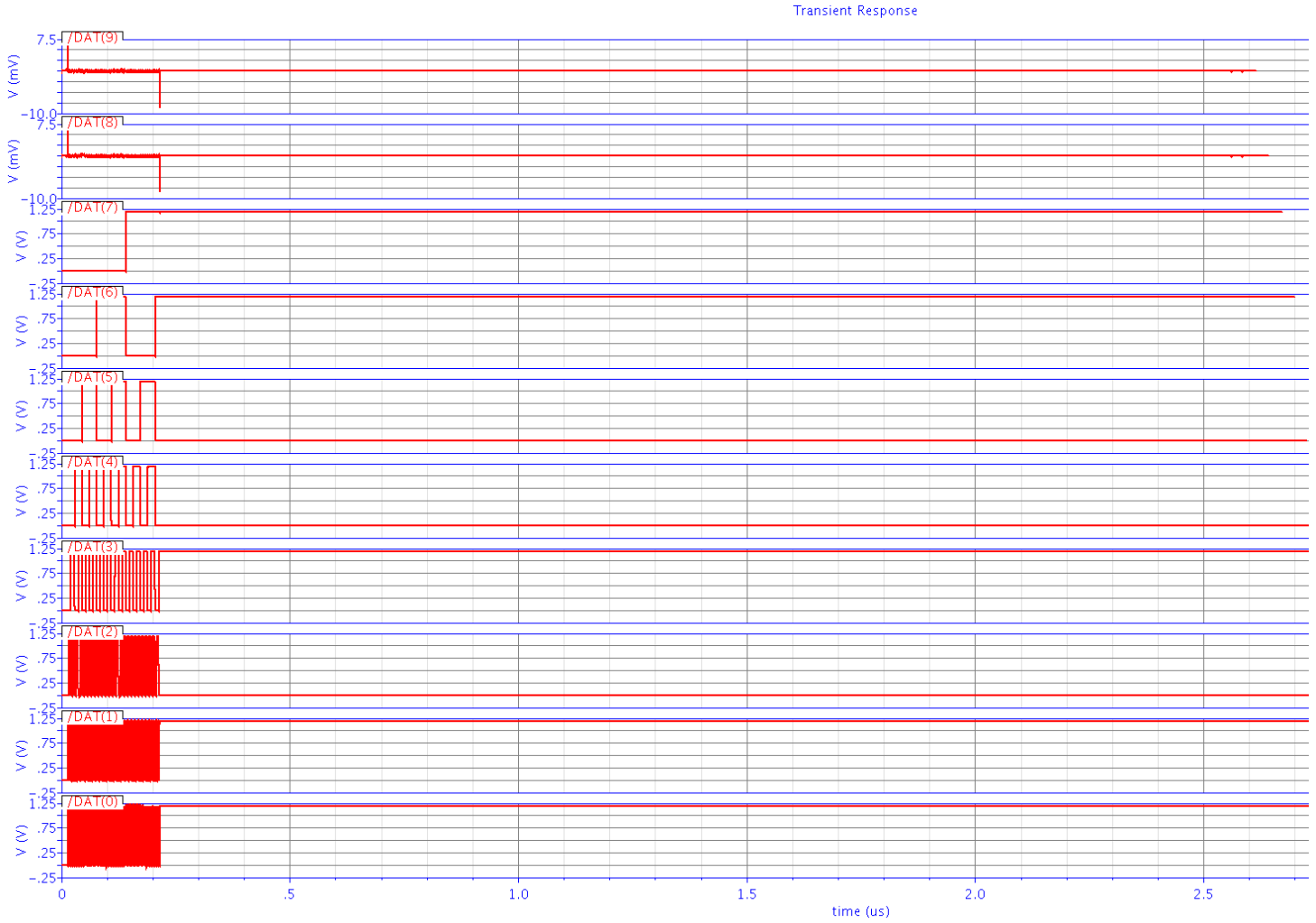
4-cell layout:



288 microns

- When running in 12 bit mode, notice of over-count given by overflow bit
- Cell's data addressed by Channel_sel & Token_sel. (more in readout slides)
- Counting and latch transparency controlled by comparator output

simulation



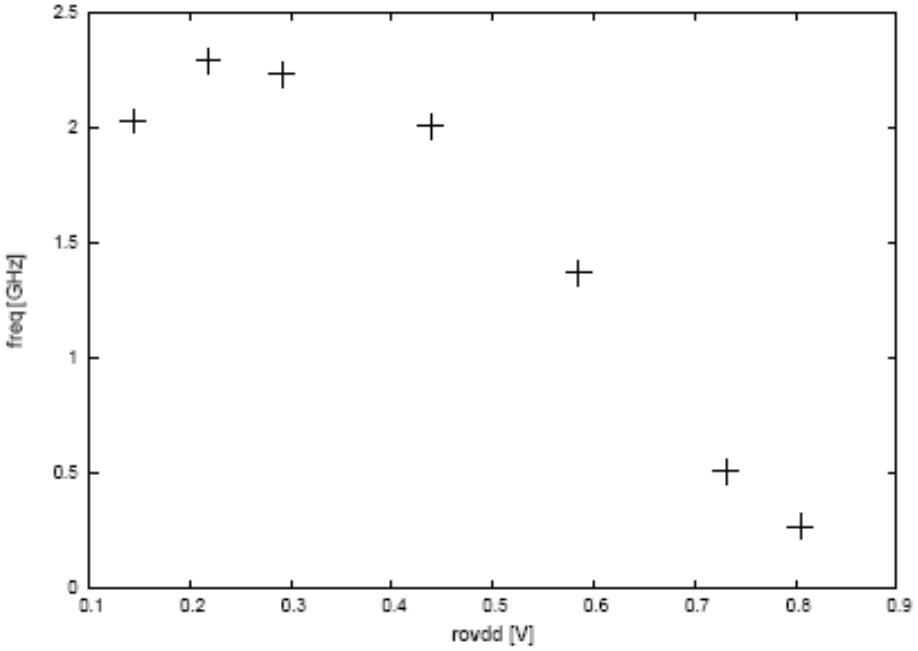
1GHz with comparator output = 200ns

DAT = 0b000011001011 ==203 counts (comparator rise+fall time)

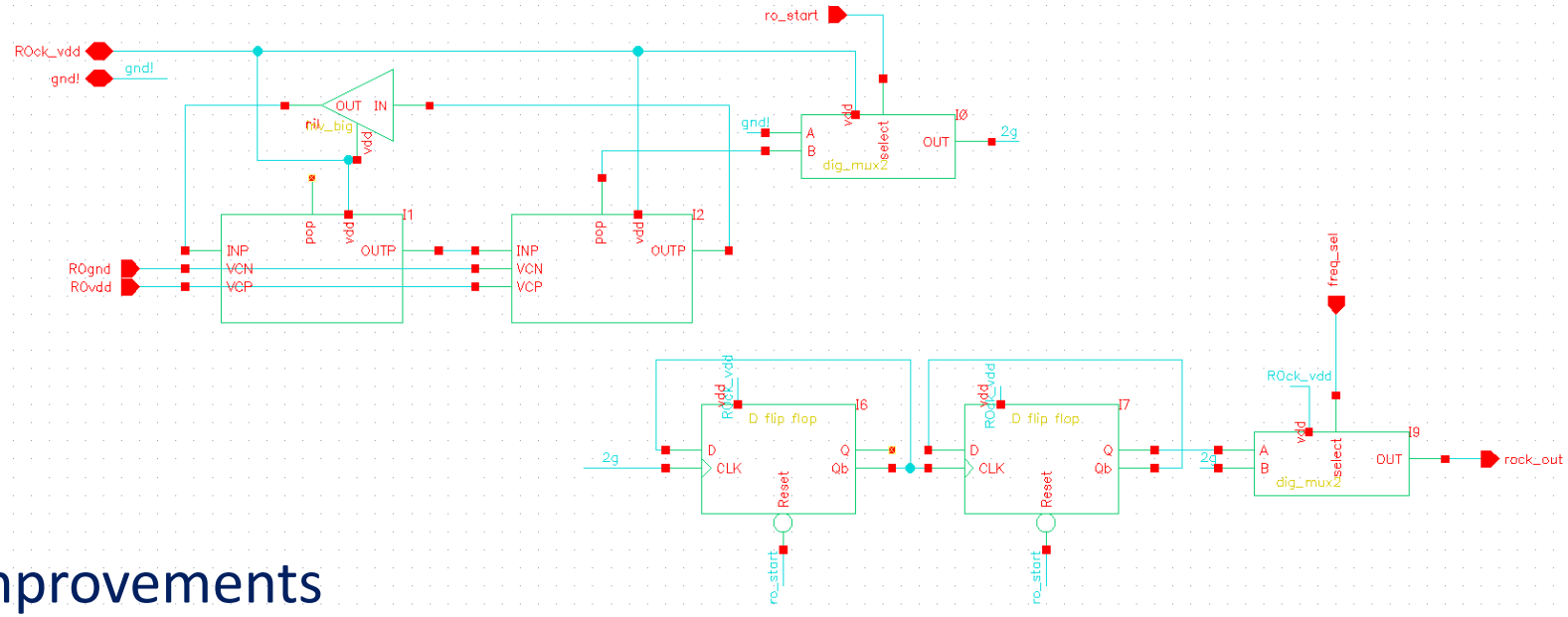
ring oscillator

- ~200MHz-2GHz clock generated on chip with ring oscillator
- 1 per channel + fan-out
- keep same structure as on PSEC2 - five stage inverter chain w/ positive feedback (analog controls on 2 stages)

Experimental results from PSEC2



ring oscillator



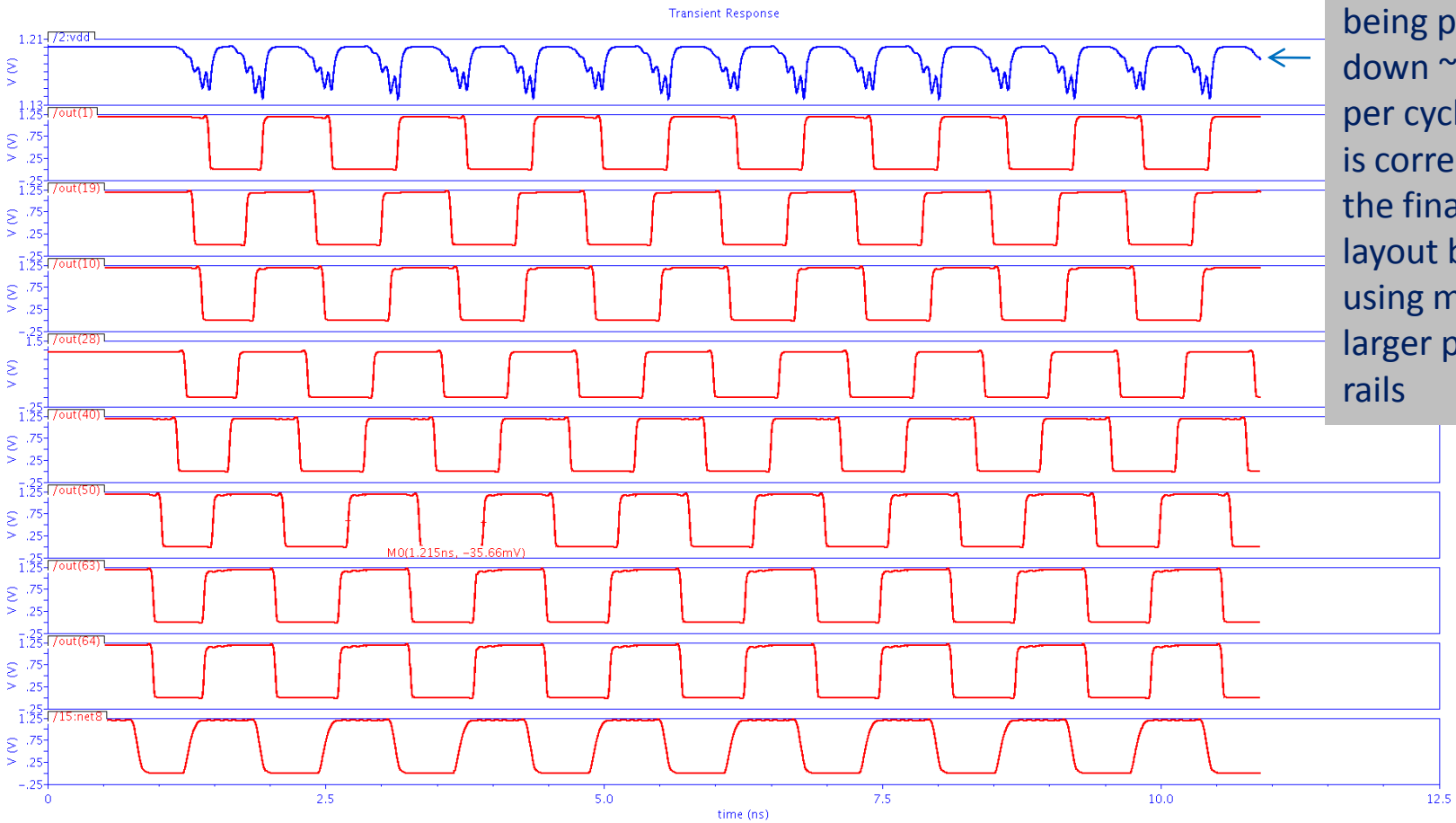
improvements

- 'frequency select' option: duty cycle of RO departs from 50% @ f<1GHz, so to run slower, send 2GHz through divide-by-4 stage. Gives clean clock up to 500 MHz.

- 'RO_enable' option: RO is free-running, but RO_en allows the fan-out drivers to be turned on/off (reducing noise).

Clock fan-out

- fully simulated post-layout. Successfully distributes RO clock to 256 cells up to about 1.8 GHz.
- drivers can be turned off during sampling to reduce digital noise



Post-layout sim @ 800MHz

Note: vdd is being pulled down ~70 mV per cycle. This is corrected in the final ADC layout by using much larger power rails

noise considerations

- ADC can be completely turned off during sampling (except for ring oscillator)

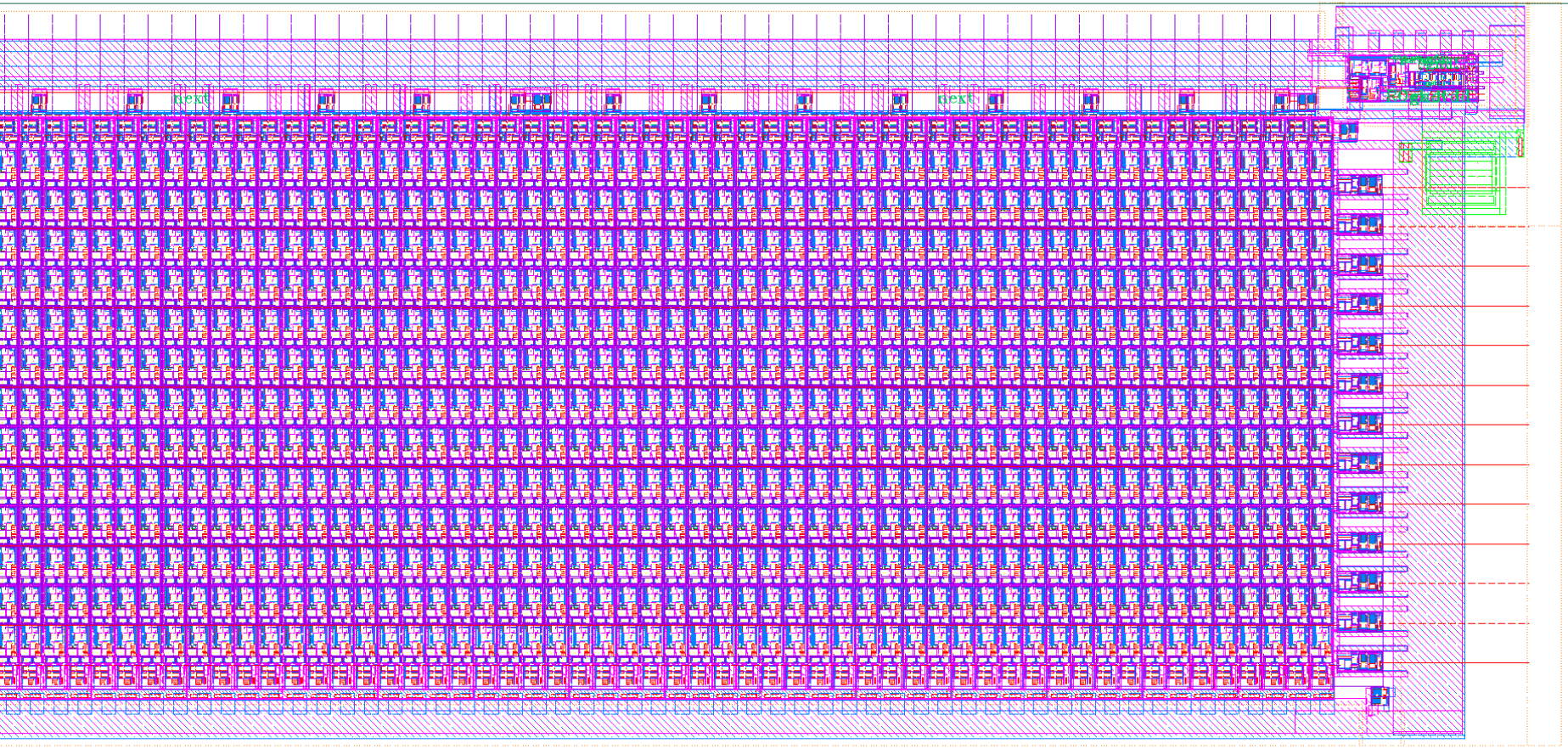
- Complete structure surrounded by a 50 micron width of BFMOAT that gives ~130 Ohms of substrate resistance between other parts of chip.

- 'Large' decoupling cap (3.5 pF) near ring oscillator

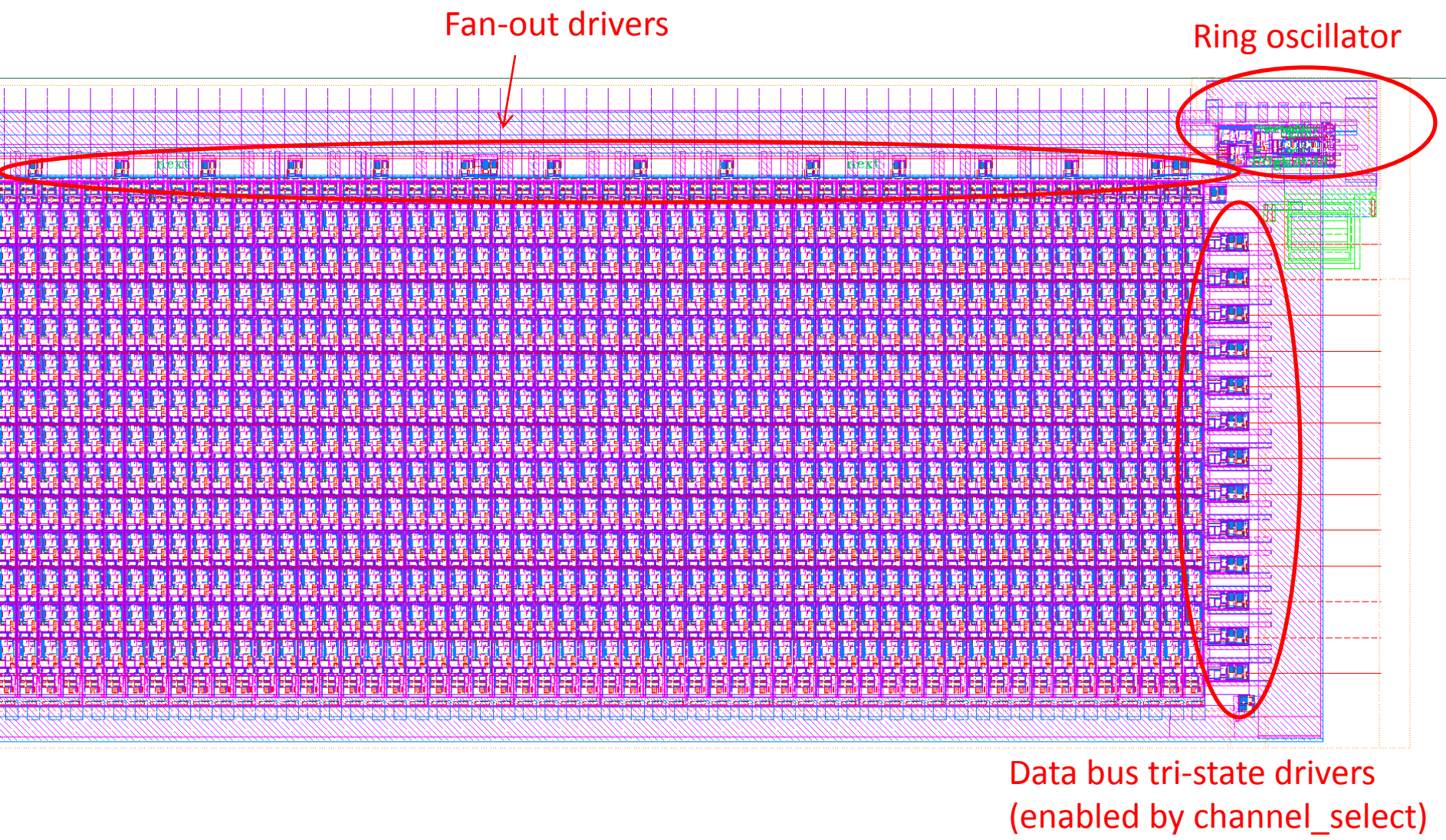
- Upon extraction, 75 pF of parasitic capacitance between vdd and gnd

- Separate power rails for ADC and analog structures

layout

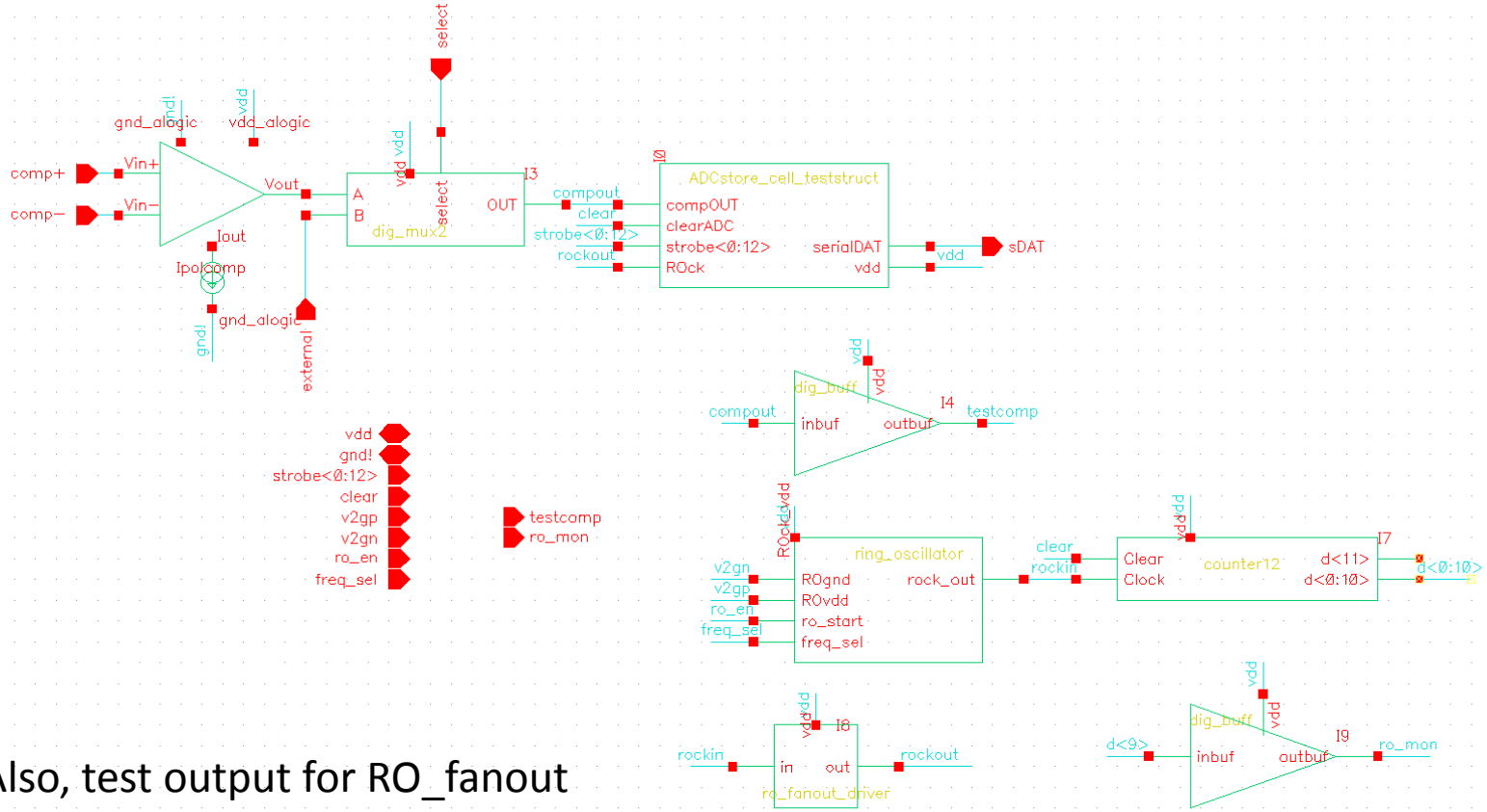


layout


Fan-out drivers
Ring oscillator
Data bus tri-state drivers
(enabled by channel_select)

Test points

- Will have ‘Test-ADC’ on chip as test structure
  - Include comparator – Ring oscillator – ADC cell
  - Test outputs: COMPout_test, RO_monitor, ADCdat_test
    - Test data will use serial readout (only one output pad needed)



- Also, test output for RO_fanout