From Chip 2 to Chip 3

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Issues with Chip 2

• ADC not functional: no way to stop the counters on a sampling cell comparator trigger. Still not understood. Post-layout simulations show supply voltage rails too small.

  The full design could not be post-layout simulated due to a prohibitive number of nodes.

• Leaks of a P transistor in the D flip-flops of the ADC counter on a floating node. Data vanish after 2\(\mu\)s.

• Signal inverted in the Trigger Logic. Had to tweak with control signals.
Addressing Chip 3 issues

• Vdd rails width increased.

• No floating node.

• Fixed the trigger logic problem.

• Added controls independent of the sampling cells.
Chip 3 design

- Six channels:
  - 4 regular sampling channels validated by the chip 2 tests
  - One timing channel (time calibration)
  - One test channel with improved sampling cell and ADC

- Improved token readout (4 blocks of 64 cells) to reduce dead time induced readout.