Comparator 1&2 and Ramp Buffer

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Comparator 1 – Schematic
Comparator gain
Comparator 1 – Layout

- Comparator size: 12µm × 22µm.
- Internal current source: 1µA.
- 6.5fF output cap.
- 1 per cell: very important offset.
Comparator 2 – Design

- The schematic of this comparator was very kindly given to us by Gerard and Jacque from LPC Clermont.
- It was modified to use less power and be smaller.
Comparator 2 – Schematic

Clocked input stage

Latch stage.
Comparator 2 – Specification

- Will be tested on 5 & 6 channels.
- Clocked comparator. The clocked used is the clock of the ADC (Ring osc – see Eric’s talk).
- Power consumption: 20uA.
- Layout not done so far.
Comparator 2 – Simulation

Working at 1GHz.
Comparator 2 gain

Transient Response

- \( V_T^{('I_{in1})} \)
- \( V_T^{('I_{in2})} \)
- \( V_T^{('clock_d')} \)
- \( V_T^{('I_{out1})} \)
- \( V_T^{('I_{out2})} \)
Ramp Buffer

- There is one ramp buffer per channel.
- Same design as the buffer for the sampling cell.
- Bigger output transistor.
- LvtPfets at the input to increase the linear range.
Ramp Buffer Schematic and Layout

Layout size: 12µm × 30µm.
Internal current source: 1µA
Driving capability

Simulation with a 10pF load.
Output integrated noise