Fast Buffer Design

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The buffering question.

- Comparator parasitics capacitance value: 3.5fF
With and without buffer

<table>
<thead>
<tr>
<th></th>
<th>Without Buffer</th>
<th>With Buffer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset</td>
<td>Offset of the comparators</td>
<td>Offset of the comparators + buffers</td>
</tr>
<tr>
<td>Noise</td>
<td>Thermic noise of the 50Ω</td>
<td>Noise of the buffer added</td>
</tr>
<tr>
<td>Readout delay</td>
<td>None</td>
<td>Buffering delay</td>
</tr>
<tr>
<td>Input dynamic</td>
<td>Maximum</td>
<td>Buffer dynamic</td>
</tr>
<tr>
<td>Linearity</td>
<td>Degraded by the parasitic capacitance of the comparator</td>
<td>Linearity of the buffer.</td>
</tr>
</tbody>
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To answer the question: buffer in 4 channels. No buffers in 2 test channels.
Buffer schematic
Fast buffer design

Characteristics:

- 14ns buffering time < 25ns of the write cycle.
- 30µV of integrated noise from 1kHz to 10GHz.
- Low power: 1µA/buffer.

- Big offset variation due to process variation (100mV measured buffer to buffer).
- 1V linear range.
Buffer Layout

- Size 12µm×16µm.
- Internal current source.
- Copy of the buffer previously implemented.
1V Linear Dynamic Range
Buffer – Rise time

Transient Response

M0(13.59ms, 977.5mV)
M2(109.8µs, -1.079V)
Buffer Noise

Total integrated noise = 120µV.
Sampling with buffer
Sampling without buffer