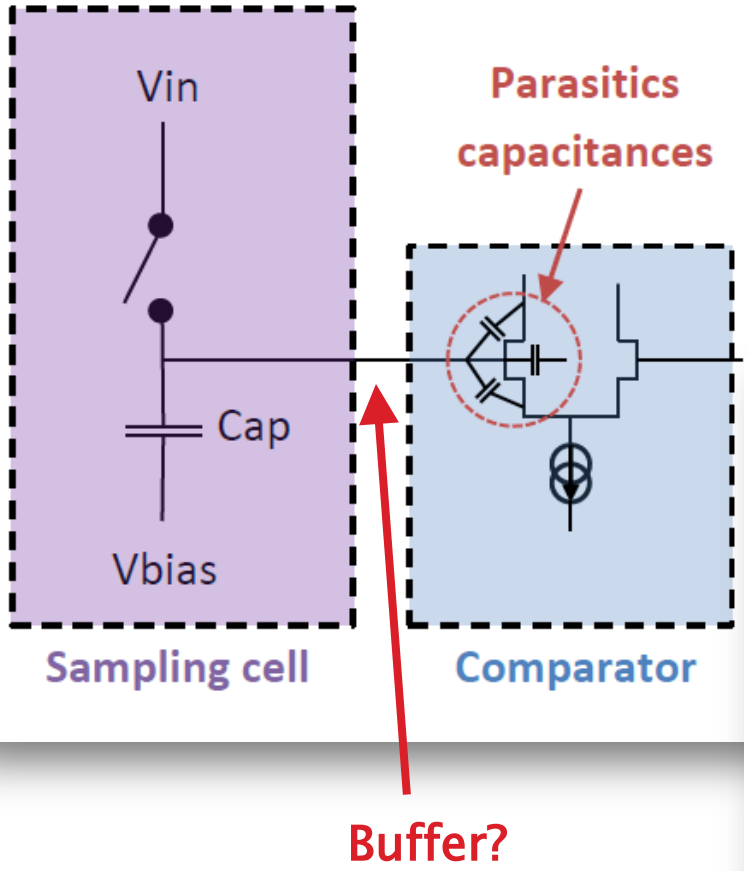
THE UNIVERSITY OF CHICAGO

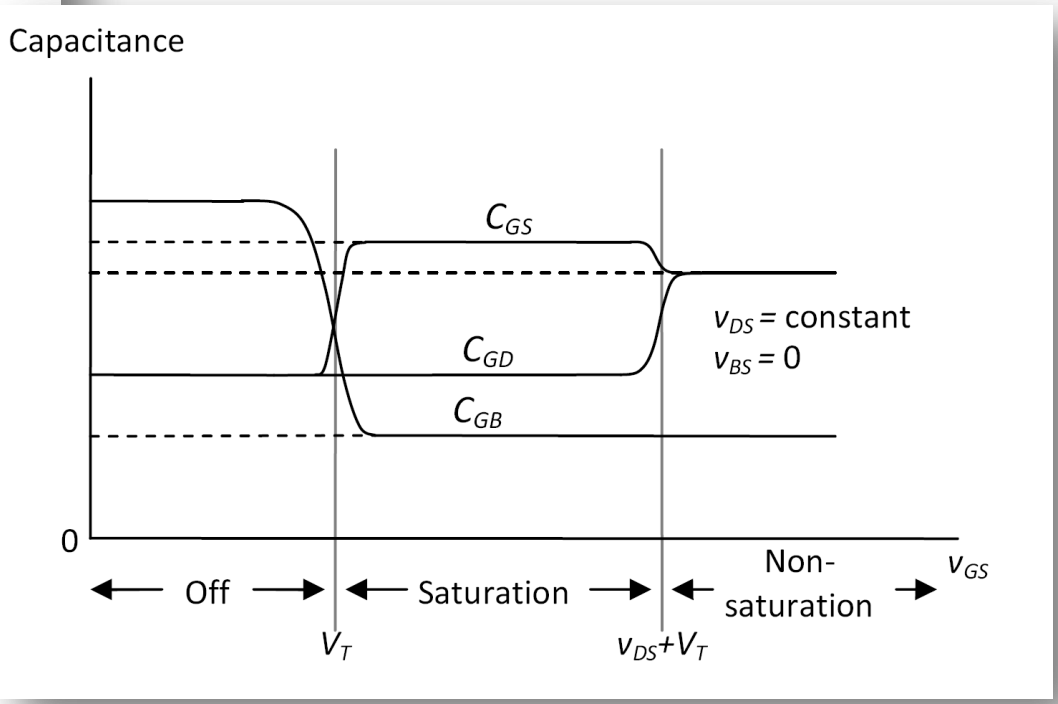
Fast Buffer Design

Hervé Grabas

The buffering question.



- Comparator parasitics capacitance value: 3.5fF

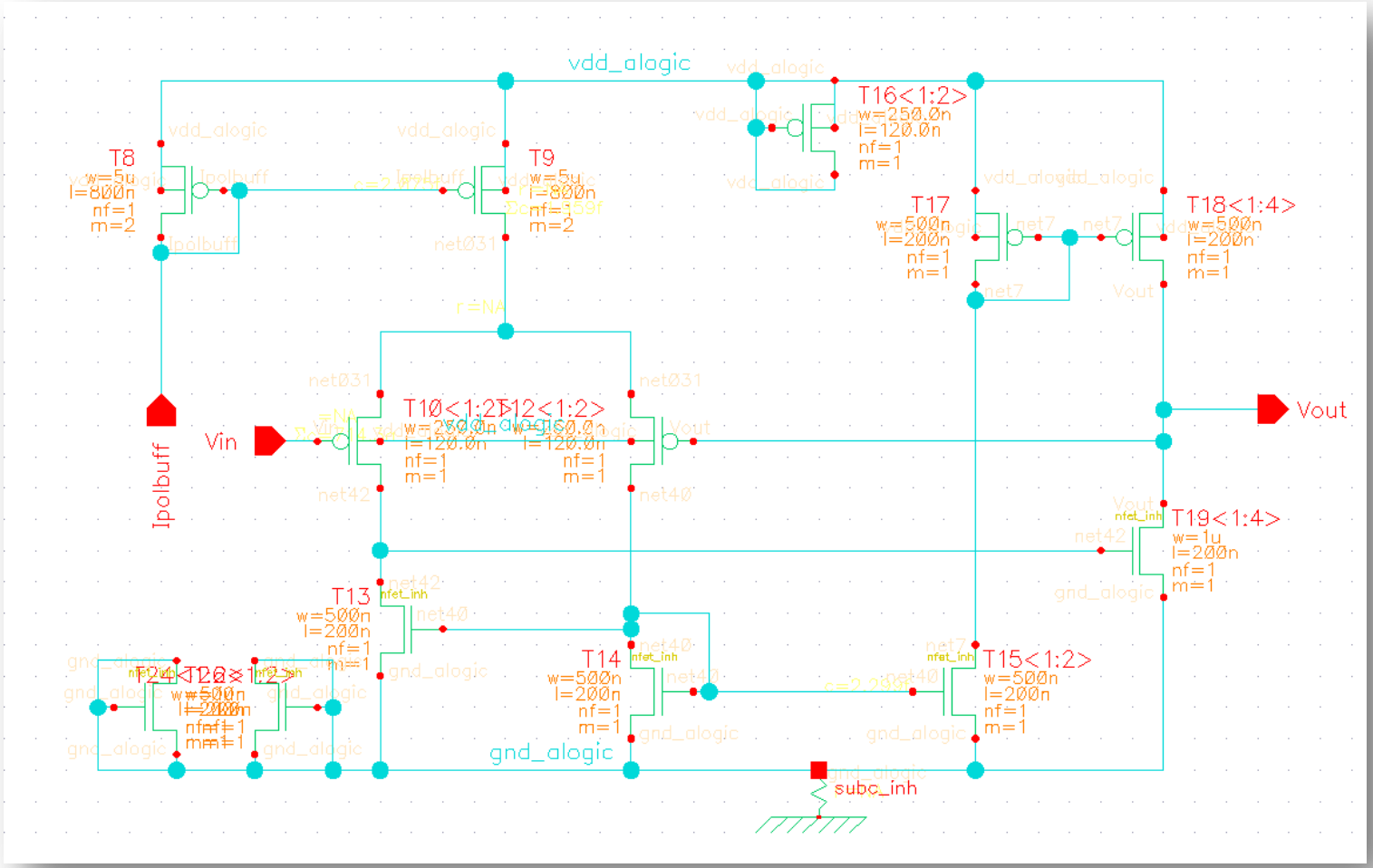


With and without buffer

	Without Buffer	With Buffer
Offset	Offset of the comparators	Offset of the comparators + buffers
Noise	Thermic noise of the 50Ω	Noise of the buffer added
Readout delay	None	Buffering delay
Input dynamic	Maximum	Buffer dynamic
Linearity	Degraded by the parasitic capacitance of the comparator	Linearity of the buffer.

To answer the question : buffer in 4 channels. No buffers in 2 test channels.

Buffer schematic

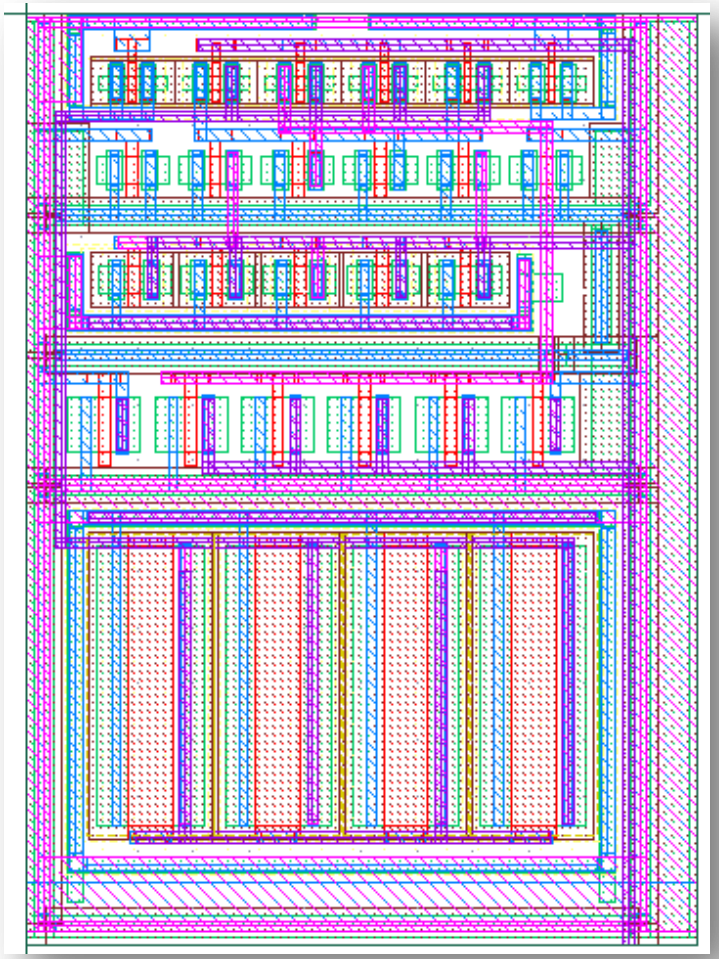


Fast buffer design

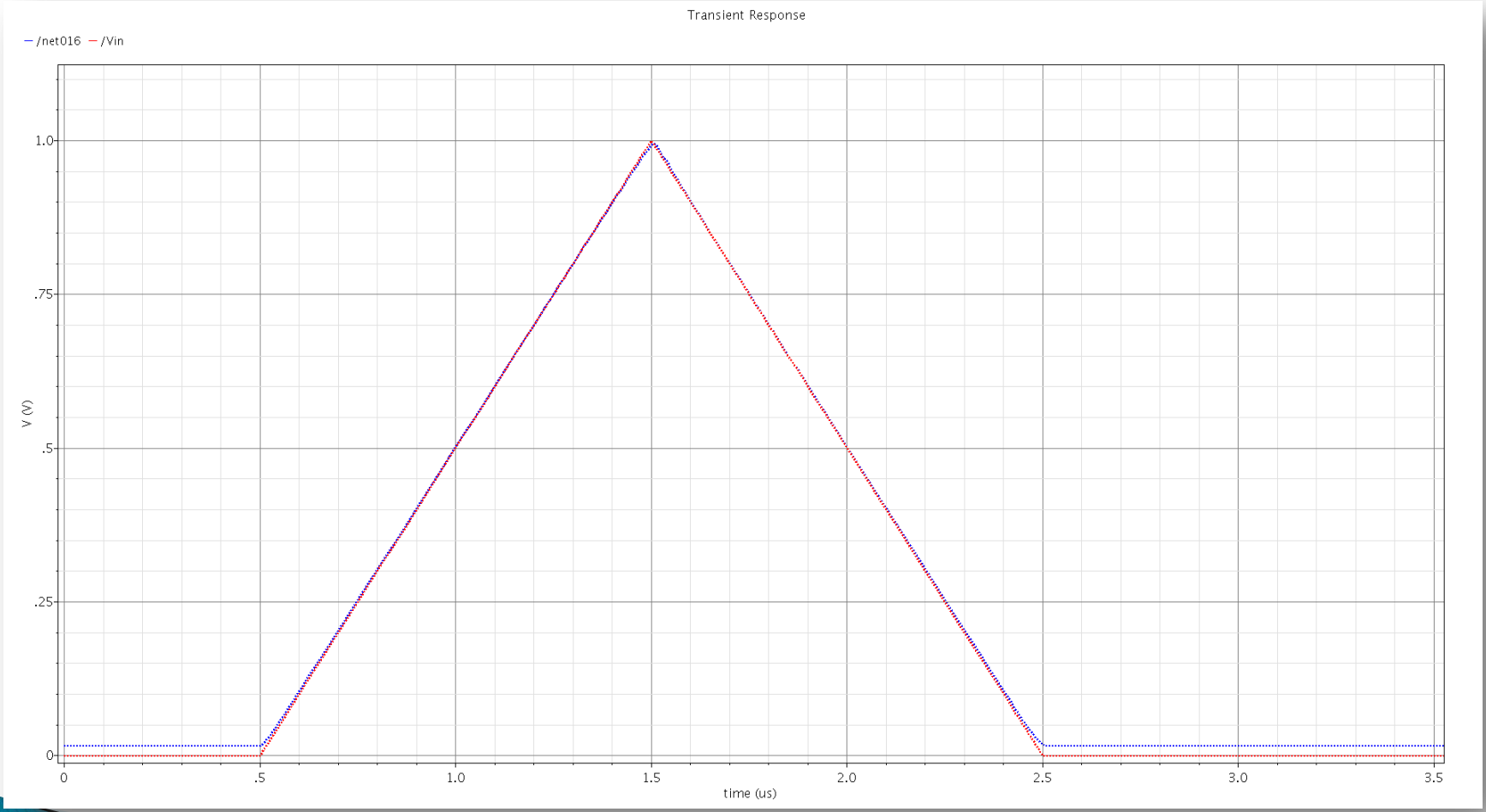
- Characteristics:
  - 14ns buffering time < 25ns of the write cycle.
  - 30μV of integrated noise from 1kHz to 10GHz.
  - Low power: 1uA/buffer.
  - Big offset variation due to process variation (100mV measured buffer to buffer).
  - 1V linear range.

Buffer Layout

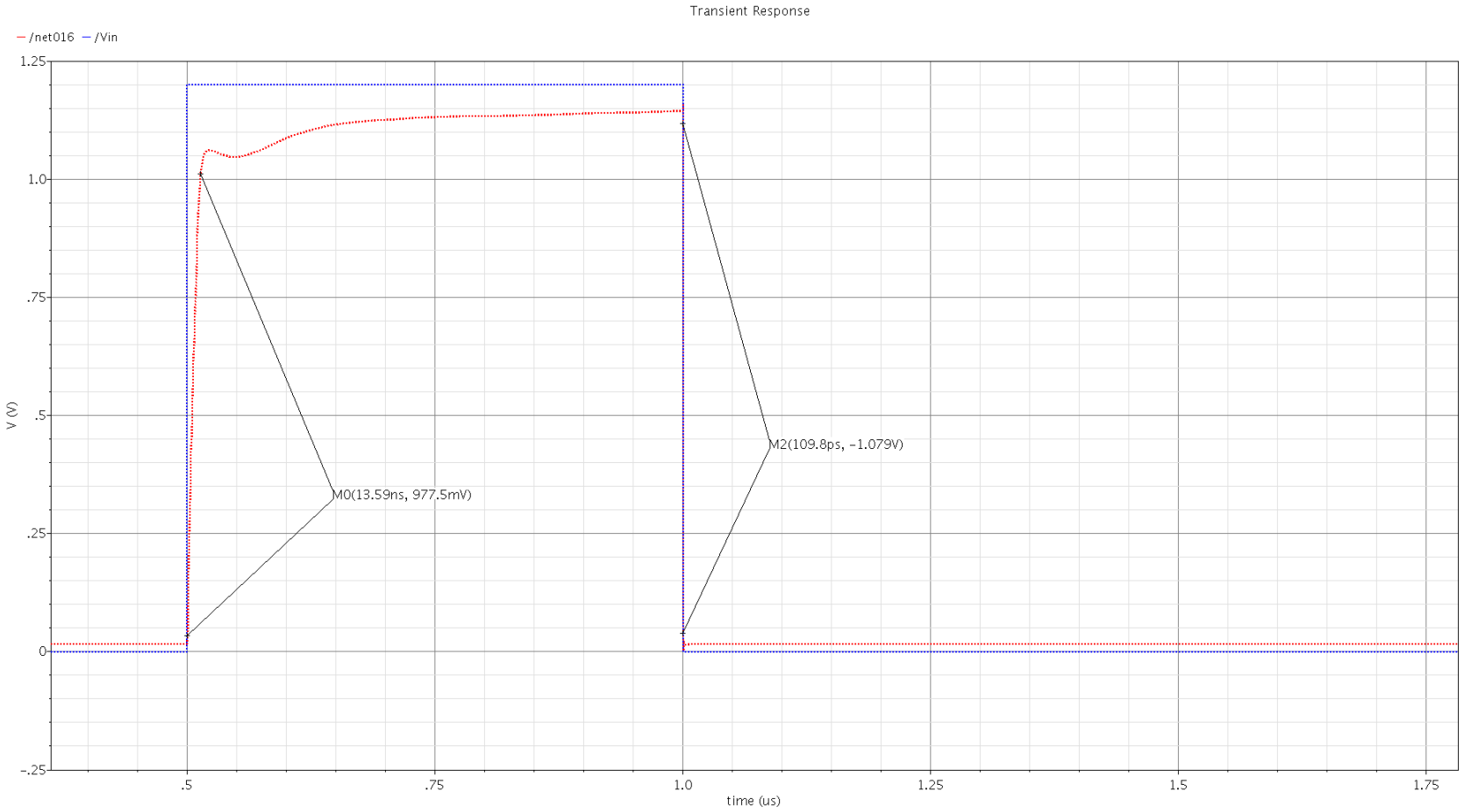
- Size 12μm×16μm.
- Internal current source.
- Copy of the buffer previously implemented.



1V Linear Dynamic Range

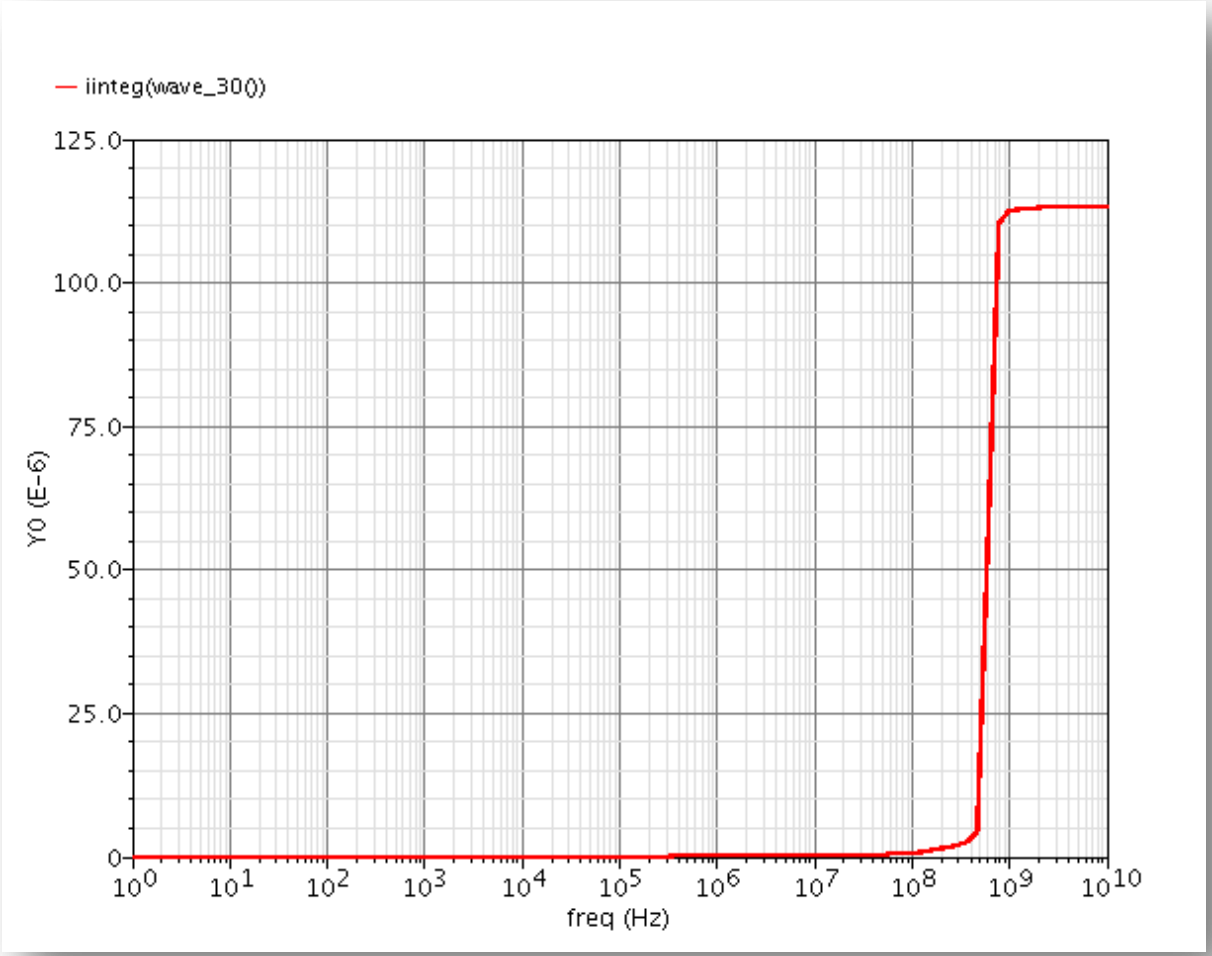


Buffer – Rise time

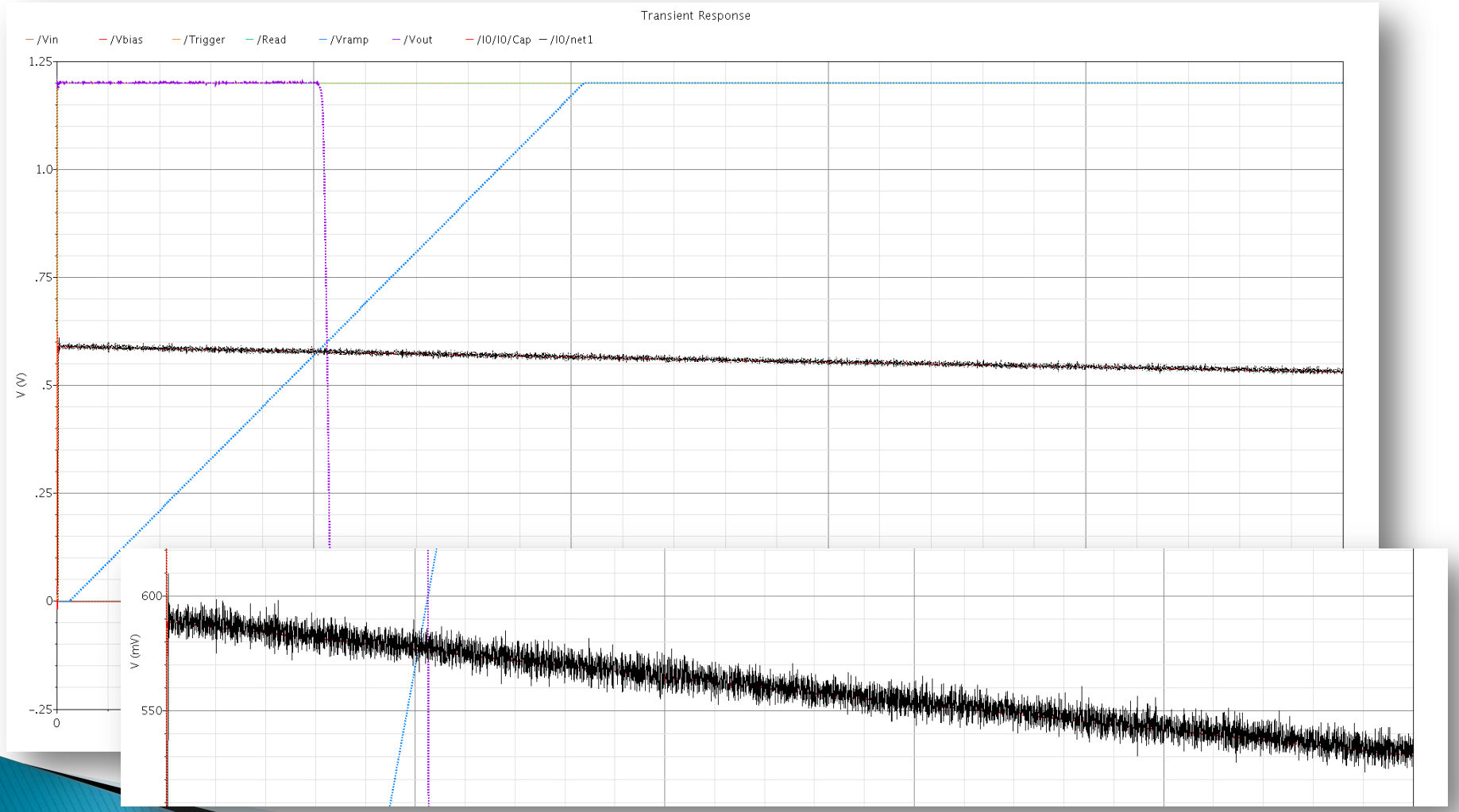


Buffer Noise

Total integrated noise = 120μV.



Sampling with buffer



Sampling without buffer