Sampling cell – Dynamic range – Analog bandwidth

Hervé Grabas
Sampling cell – Principle

- An unit is basically made of one storage capacitance controlled by two signals:
  - Timing (800ps wide pulse).
  - Trigger (in case of an event).
- Timing stores the analog values in the sampling capacitance at a rate of 15Gs/s.
- Trigger open all the write switches in case of an event at the input.

Nota: in case of this diagram Timing is active high.
Sampling cell – Input switch size

- Input switch size: 10µm $\times$ 120nm.
The Ron resistance is Voltage dependent. Therefore the rise time will be amplitude dependent inside the cell. Ron ~ 100Ω
Switch leakage

Voltage drop: 35mV in 3us. Leakage current: 600pA.
Sampling cell – Capacitance

- Sampling capacitance: 60fF after extraction.

- Interdigitated layout with three levels of metals (M1, M2, M3).

- Shielding
  - Top shielding in MQ.
  - Side shielding in M1, M2, M3, MQ.
Input line improvements

- Went from M3 to MQ (gain a factor 2 in lin.res.).
- Add anti-fill layers, for layers from M1 to MG.
- Increase the width.
Separate analogic vdd and analogic gnd.

Regenerative buffers for every input signals (Timing, Trigger, Read, Write).
Sampling cell – Layout

- Size: 12µm × 55µm.
- Input line in MG: 800nm × 3.072mm.
- Input line resistance: 38µΩ/□.
- Total input line resistance: 146Ω.
- Total input line capacitance: 1.5pF (without including the pad).
- The sampling has 2 poles:
  - \( \frac{1}{(2 \times \pi \times 50\Omega \times 1.5pF)} = 2GHz \) (input line)
  - \( \frac{1}{(2 \times \pi \times 100\Omega \times 60fF)} = 20GHz \) (sampling cap)
50ps rise time (7GHz bwt). The limitation is at the input.
The 50Ω input resistance

- The input line coming from the detector is a 50Ω transmission line.
- There is three possibilities for the terminaison:
  - On board
  - On chip after the pads
  - On chip at the end of the 256 cells.
The 50Ω input resistance (2)

<table>
<thead>
<tr>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>On the board</strong></td>
<td></td>
</tr>
<tr>
<td>• Can be replaced</td>
<td>• The pad capacitance ~3pF and input line cap ~1.5pF are in series with 50Ω.</td>
</tr>
<tr>
<td>• Possibility of a good transmission line</td>
<td>• Bwth &lt;1GHz</td>
</tr>
<tr>
<td>until the terminaison.</td>
<td></td>
</tr>
<tr>
<td><strong>After the pad</strong></td>
<td></td>
</tr>
<tr>
<td>• Input signal won’t see the pad input cap.</td>
<td>• Non replaceable.</td>
</tr>
<tr>
<td>• Bandwidth 1–2GHz.</td>
<td>• More impedance mismatch at the input of the chip.</td>
</tr>
<tr>
<td><strong>After the transmission line</strong></td>
<td></td>
</tr>
<tr>
<td>• Maximum bandwith possible.</td>
<td>• Non replaceable</td>
</tr>
<tr>
<td></td>
<td>• Potentiel drop of tension across the input line (Res = .1Ω) ?</td>
</tr>
</tbody>
</table>
The 50Ω input resistance

- 4 channels with 50Ω outside the chip.
- 2 test channels with 50Ω at the end of the line.