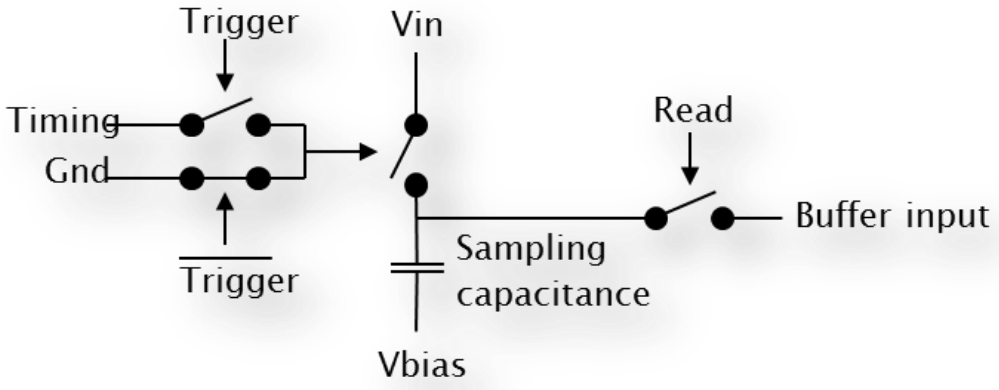
THE UNIVERSITY OF CHICAGO

Sampling cell – Dynamic range – Analog bandwidth

Hervé Grabas

Sampling cell – Principle

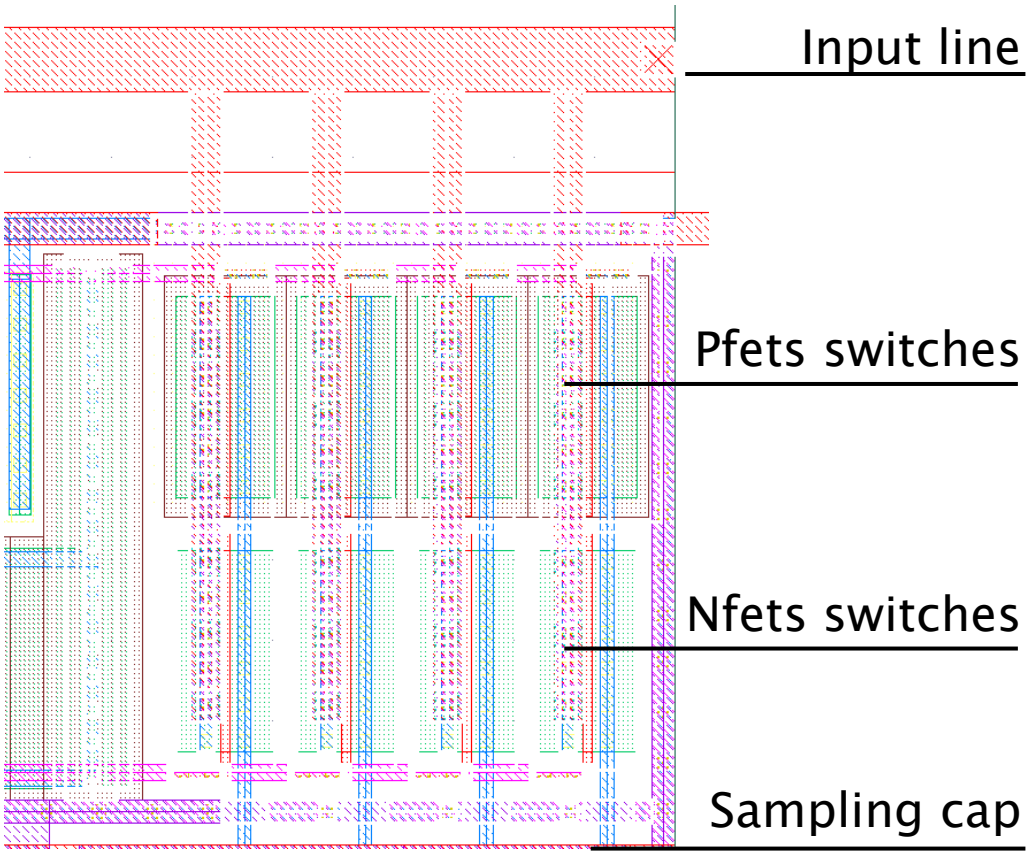
- An unit is basically made of one storage capacitance controlled by two signals :
  - –Timing (800ps wide pulse).
  - –Trigger (in case of an event).
- Timing stores the analog values in the sampling capacitance at a rate of 15Gs/s.
- Trigger open all the write switches in case of an event at the input.



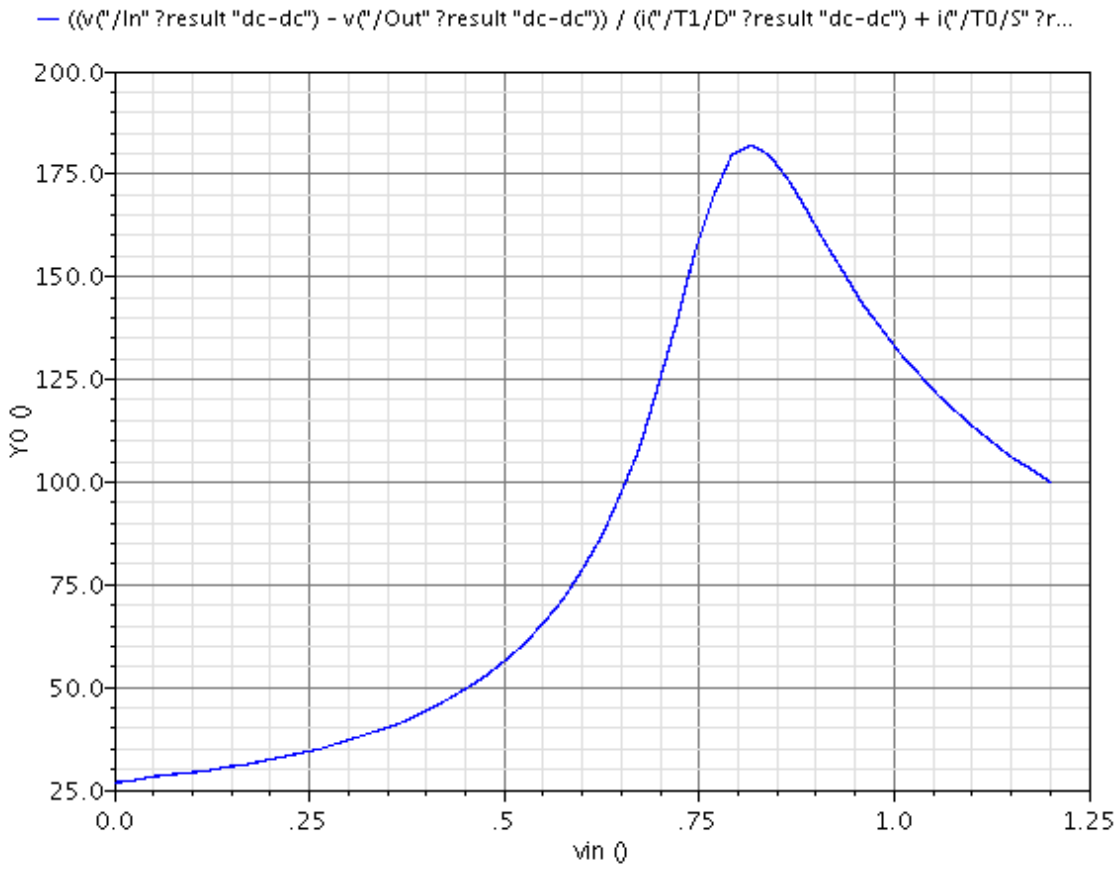
Nota: in case of this diagram Timing is active high.

Sampling cell – Input switch size

- Input switch size: 10μm×120nm.

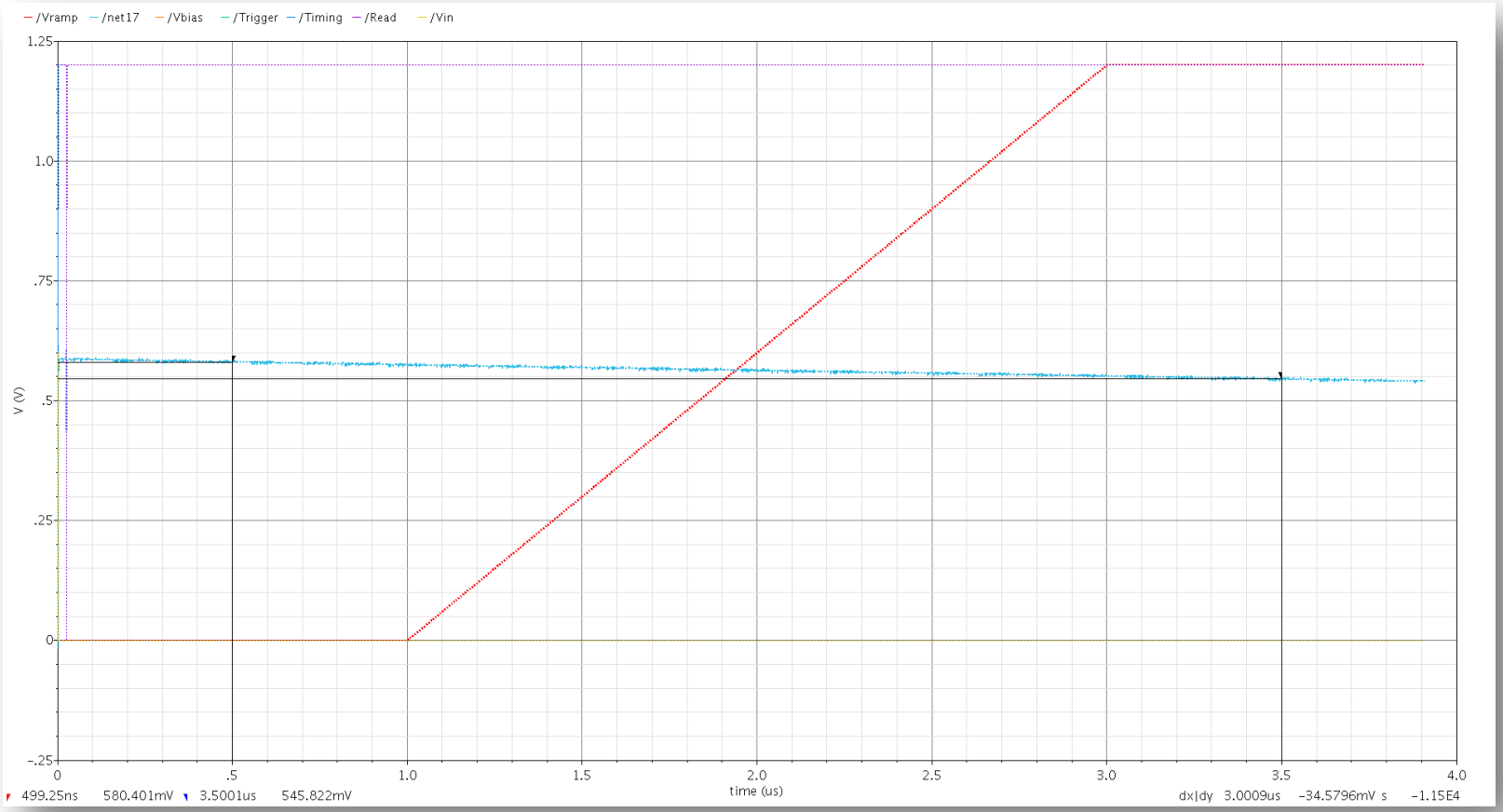


Sampling cell – Input switch Ron



The Ron resistance is Voltage dependent. There fore the rise time will be amplitude dependent inside the cell. Ron ~ 100Ω

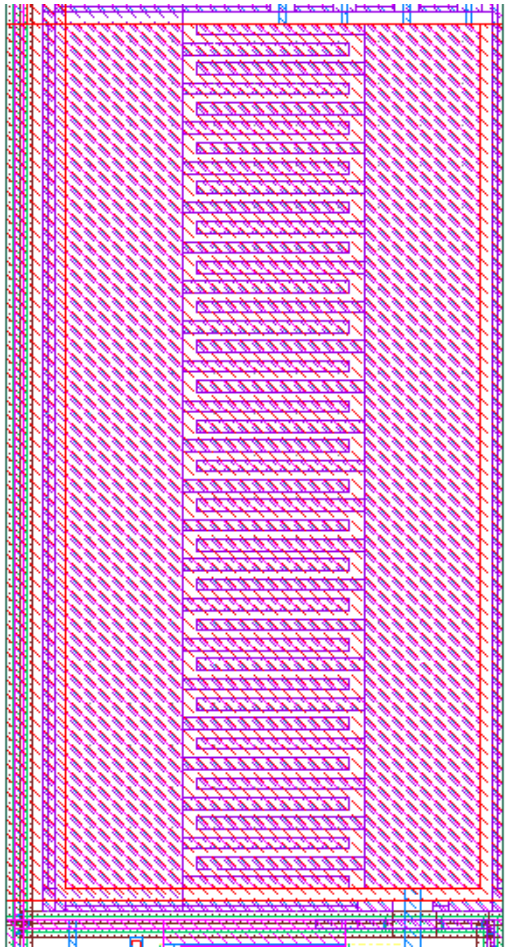
Switch leackage



Voltage drop: 35mV in 3us.
Leackage current: 600pA.

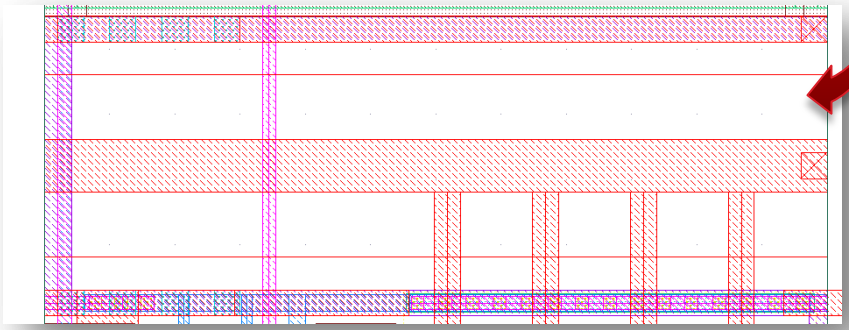
Sampling cell – Capacitance

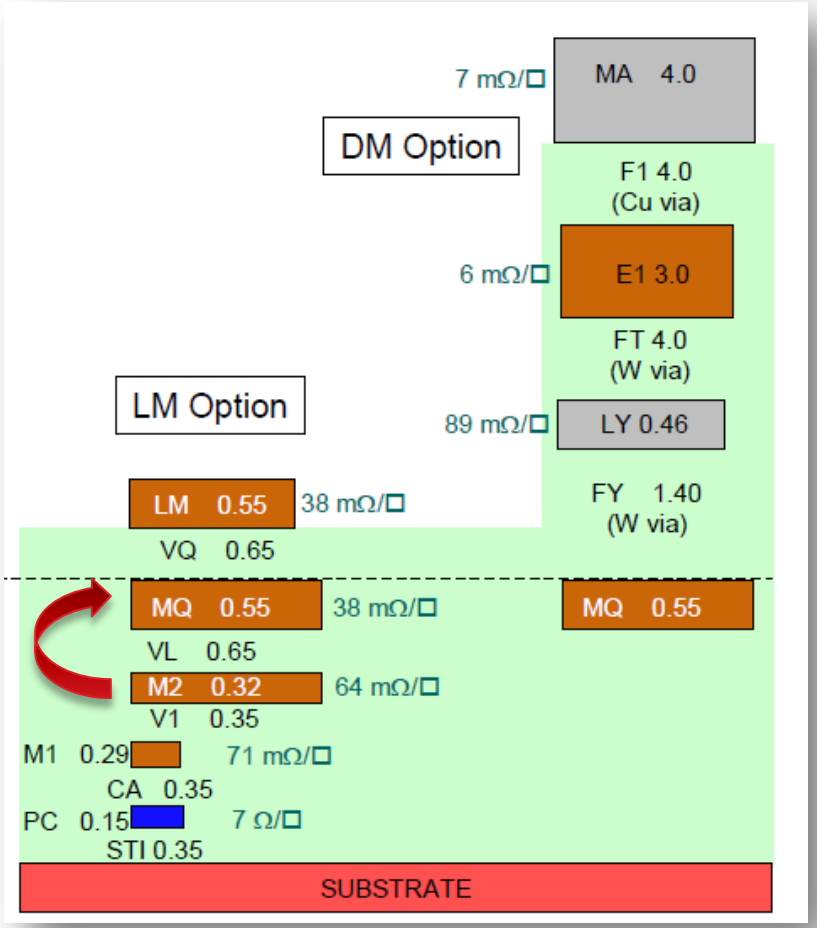
- Sampling capacitance: 60fF after extraction.
- Interdigited layout with three levels of metals (M1, M2, M3).
- Shielding
  - Top shielding in MQ.
  - Side shielding in M1, M2, M3, MQ.



Input line improvements

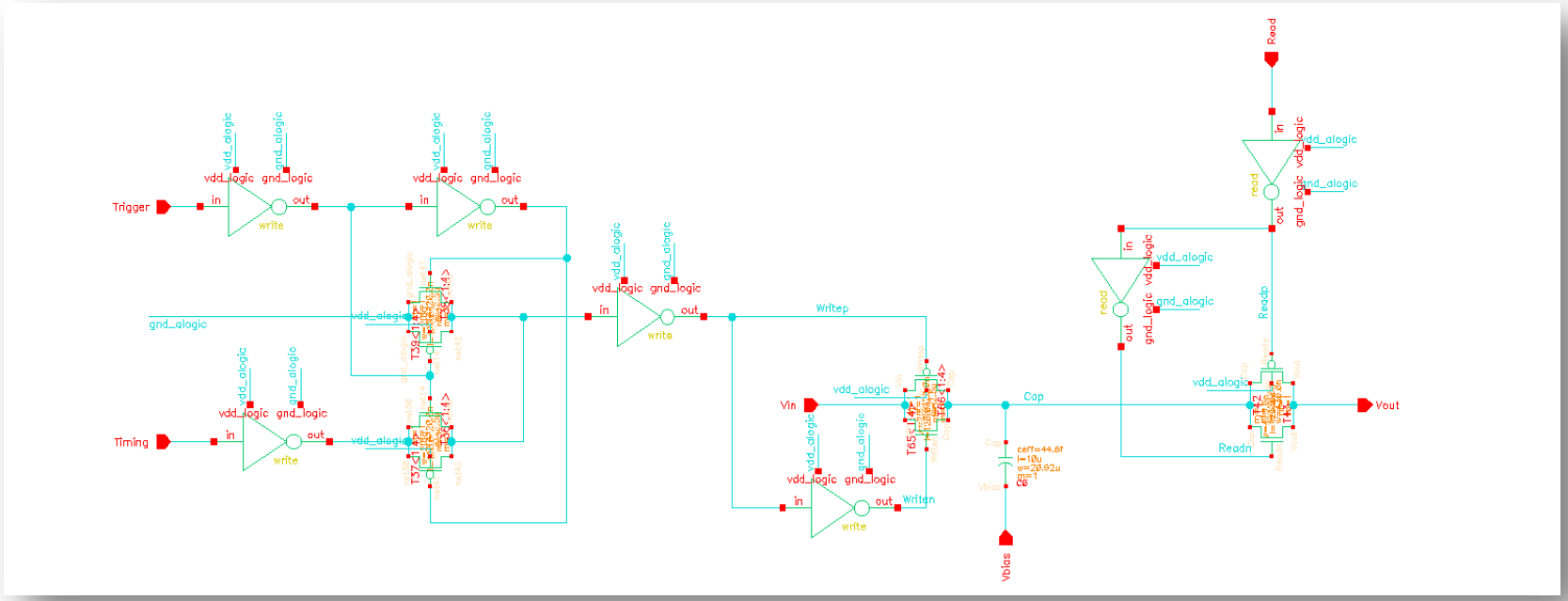
- Went from M3 to MQ (gain a factor 2 in lin.res.).
- Add anti-fill layers, for layers from M1 to MG.
- Increase the width.





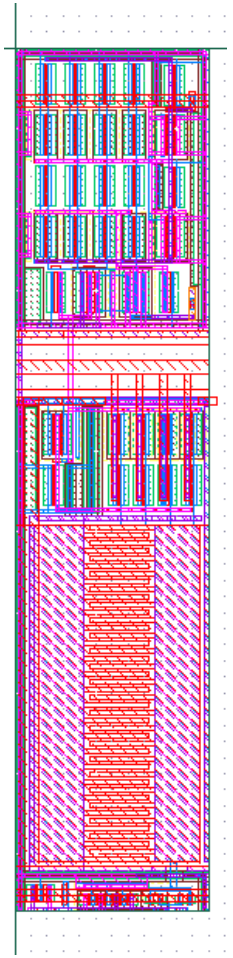
Sampling cell – Schematic

- Separate analogic vdd and analogic gnd.
- Regenerative buffers for every input signals (Timing, Trigger, Read, Write).

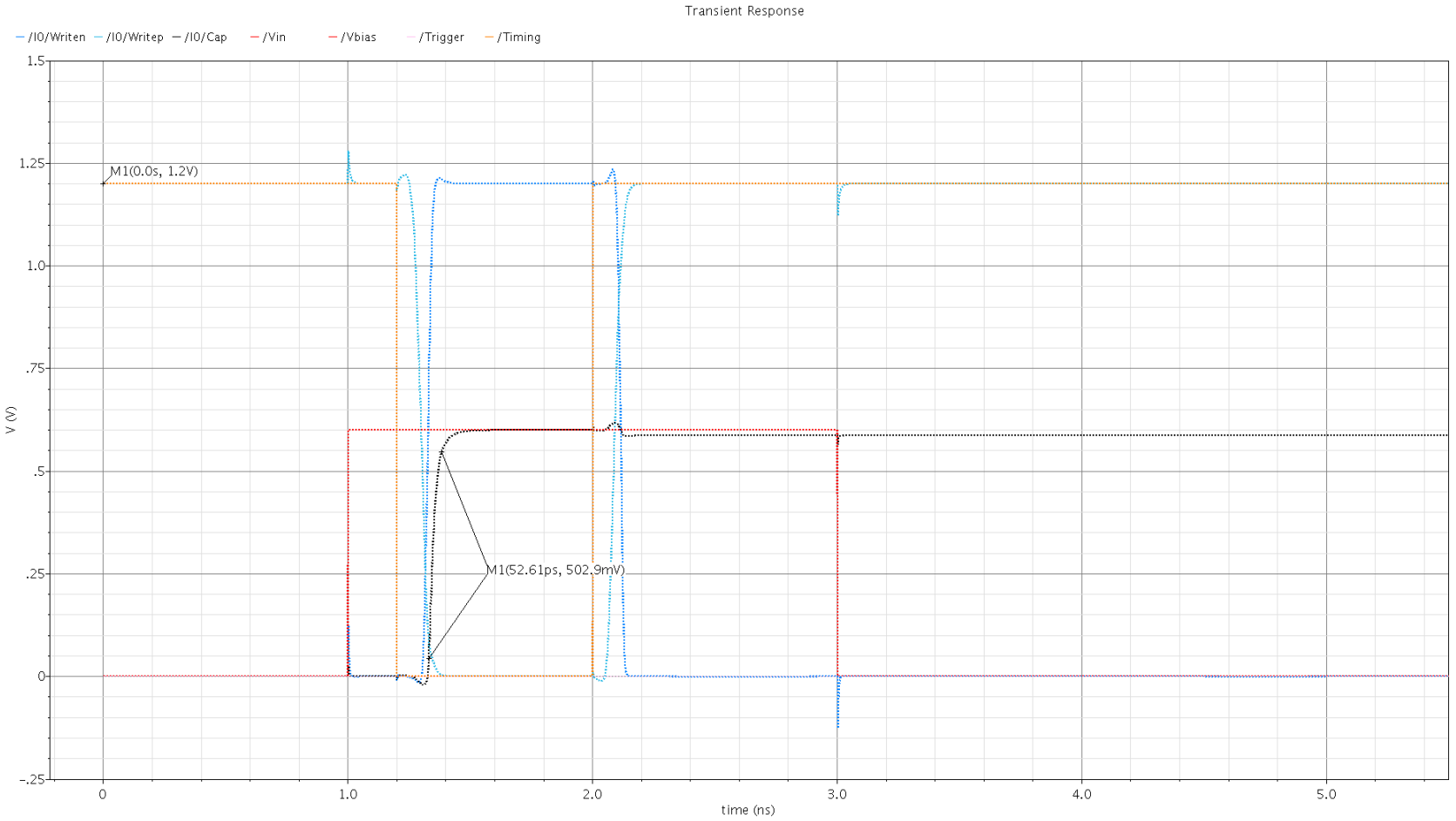


Sampling cell – Layout

- Size:12μm×55μm.
- Input line in MG : 800nm×3.072mm.
- Input line resistance: 38μΩ/□.
- Total input line resistance: .146Ω.
- Total input line capacitance: 1.5pF (without including the pad).
- The sampling has 2 poles:
  - 1/(2×π×50Ω×1.5pF) = 2GHz. (input line)
  - 1/(2×π×100Ω×60fF) = 20GHz. (sampling cap)



Sampling cell – Simulations



50ps rise time (7GHz bwt). The limitation is at the input.

The 50Ω input resistance

- The input line coming from the detector is a 50Ω transmission line.
- There is three possibilities for the terminaison:
  - On board
  - On chip after the pads
  - On chip at the end of the 256 cells.

The 50Ω input resistance (2)

	Advantages	Disadvantages
On the board	• Can be replaced • Possibility of a good transmission line until the terminaison.	• The pad capacitance ~3pF and input line cap ~1.5pF are in series with 50Ω. • Bwth <1GHz
After the pad	• Input signal won't see the pad input cap. • Bandwidth 1-2GHz.	• Non replaceable. • More impedance mismatch at the input of the chip.
After the transmission line	• Maximum bandwith possible.	• Non replaceable • Potentiel drop of tension across the input line (Res = .1Ω) ?

The 50Ω input resistance

- 4 channels with 50Ω outside the chip.
- 2 test channels with 50Ω at the end of the line.