10-20 GS/s Sampling chip V4

-1 Specifications.

Channels	4 + 1 test + 1 timing
Sampling rate	10-20 GS/s
Analog Bandwidth	1-2GHz
Self or External trigger	
Dynamic range	800mV
Sampling window	400ps-800ps (or 8 delay cells)
Sampling jitter	10ps
Crosstalk	1%
DLL Timing generator	Internal phase comparator and charge pump, external LP filter
DC Input impedance	½ 50Ω internal, ½ external
Conversion clock	Adjustable 500MHz 1GHz internal ring oscillator. Maximum conversion time 8us.
Read clock	40 MHz. Readout time (4-channel) 4 x 256 x 25ns=25.6 μs
Power	40mW/channel
Power supply	1.2V
Process	IBM 8RF-DM (130nm CMOS)

-2 I/Os

Signal Name	Type	I/O Pad	Function
SCA Channels Inputs			
signal0-4	aI		Analog inputs 0-1V, 50Ω to returns vbias0-4
vbiasl0-4	aI		Input return
thresh0-4	aI		External Channel Triggers thresholds

Channel common digital signals			
COMPbypass_sel	dI		Selects the latch of the ADC counters. Low: Latch_EXT, High: sampling cell comparator's output.
Latch_EXT	dI		External Latch of the ADC counters (regular is sampling cells comparator's outputs)
READswitch_cntrl	dI		Read switch control. Enables the sampling cell voltage onto the sampling cell comparator.

TRIGsign	dI	Threshold on negative or positive input transition.
TRIGen	dI	Selects internal or external trigger
TRIG	dI	High: freezes the voltage on the sampling caps. Low: the fixed sampling window (8 delay cells) on channels 0 and 1, the variable sampling window on channels 2-4 to controls the sampling cells
RO_en	dI	Enables the RO frequency divider (1:4) to clock the ADC.
RAMP	dI	Enables the ramp (active low). Clears Cext when high.
ClearADC	dI	Resets the ADC counters.
ClearTRIG	dI	Clears the internal triggers responses.
RESET_DLL	dI	Resets the DLL's timing generator control voltages
RO_freq_sel	dI	Selects the ADC clock frequency (divide 1 or 4)

Analog Voltages/currents

TRIGbias	aI	Bias current for the input comparators (triggers).
CEXT	aI	External capacitor (RAMP)
RAMPbias	aI	Controls the ramp current (slope).
V2GN	aI	Controls the ADC ring oscillator frequency clock falling edge
V2GP	aI	" " leading edge
VswN	aI	Controls the sampling window falling edge
VswP	aI	" leading edge
biasDLL_1	aI	Controls the charge pump "ups"
biasDLL_2	aI	" "downs"
Ipol1	aI	Controls Charge pump for DLL falling edge
Ipol2	aI	" " rising edge
COMPin_test+	aI	Test comparator input +
COMPin_test-	aI	" -

Clocks/Readout

WriteCLK	dI	Write clock (40 MHz to timing generator)
Copy_CLKin	dI	Copy of Write clock
Rd_ck-1-2	dI	Read clocks (40 MHz)
Tok_in-1-2	dI	Inputs of the token passing
CHIP_oe	dI	Chip output enable (12 data bus). Active low.
D0-11	dO	12-bit data bus controlled by the tokens (see below) and the Channel decoder outputs.Tied to ground in the Hi-Z state with a large internal resistor.
Overflow	dO	ADC's counters overflo

tokout-1-2	dO	Output of the token passing

21

Test outputs

ROmonitor	dO	Bit #9 of the ADC counter (divide frequency by 1024)
SerialDAT_test	dO	Serial test data output (ADC's counter + overflow) available on token 2 65-77
COMPtest	dO	Test comparator output
ROfan_test	dO	Test counter 9th bit buffered output
RAMP_buffer_out	aO	Ramp test output

5

Trigger outputs

TRIGout_0-4	dO	Channel Triggers inputs.
Trigger_or_out	dO	OR of the Channel Triggers outputs

6

DLL outputs

VDL_out	dO	Output from VCDL for delay lock
VCN_out	aO	Rising edge analog output control
VCP_out	aO	Falling edge analog output control

3

Channel and Token controls address Decoders

ChanX-Y-Z	dI	Channel address, selects the channel to be read. 0 no channel selected 1-5 channel 1-5 6 clear the ring oscillator monitor counter 7 xx (or channel 6 if implemented)
TokX-Y-Z	dI	Token control. Readout as 4 blocks of 64/channel (to skip known off-time data)

0 no block selected,
1-4 token block 1-4
5 clear token
6 clear trig

6

Power supplies

Vdd	+1.2V
Gnd	0V

Chip:

81 I/Os
22 Gnd
16 Vdd

119 pads (one unused)

Package CQFP120B:

120 pads

All analog inputs protected with DC path to Gnd and Vdd +/- .6V (5 x 10 μm2 diodes).

-3 Operation Modes

Modes

Write Writes continuously samples of inputs in 60 fF sampling caps arrays at 10-20 GS/s for 25=12.5 ns. Sampling stopped upon internal or external trigger.

Conversion Clears 2 GHz counter, ramps up Wilkinson ADCs for 2 μs.

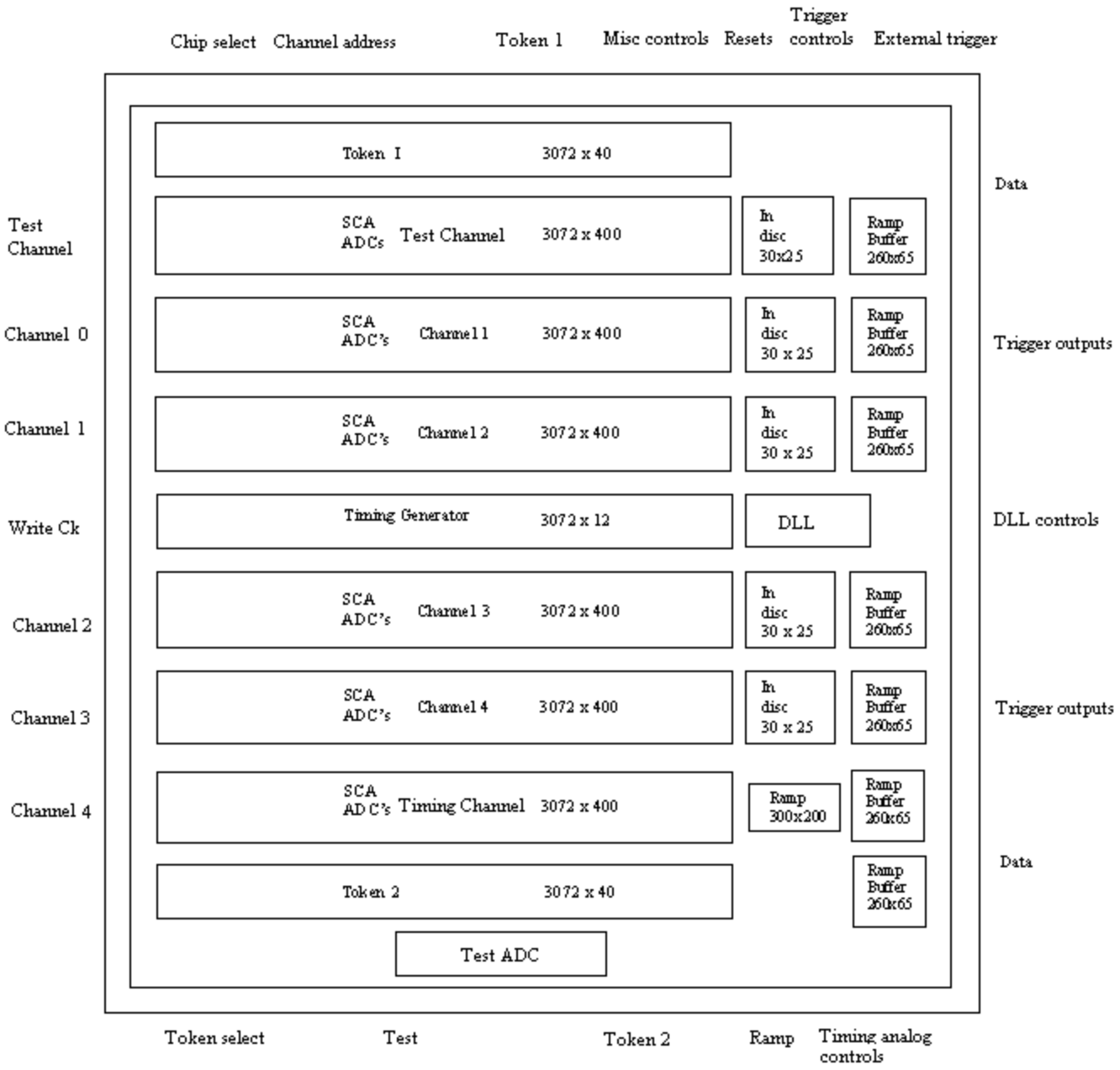
Read Sequences 256 counters of the channel selected by Chan-0-3 onto the data bus at 40 MHz read clock rate. Readout can be partitioned into four blocks of 64 caps (token readout) for each channel. Token controlled by three bits (see above)

Test structures

Test structure including a full 12-bit ADC. Outputs read sequentially using the token 2 control.

-4 Layout (to be updated)

Blocks sizes:	Timing generator	10 x 12	μm2	x 256
	Sampling cell	12 x 100		“
	Input comparator	30 x 25		x 4
	Comparator	12 x 30		x 256
	Counter	12 x 300		“
	Token	12 x 40		“
	Ramp	100 x 300		
	Ramp buffer	260 x 65		
	Ring Oscillator	12 x 50		
	Divider	12 x 300		



Size: 4500 x 4500 μm2