PSEC2 ASIC tests

6/29/2010
Updated: 8/1/2010

eric oberla
PSEC2 Eval Board
Ring Oscillator – digitization speed

Ramp generation
Channel 1 – Analog out (DC level)

Sampling rate: 5GS/s          readout speed: 125KHz (8 us/cell)

dips every 512 us due to pause in readout (output bus in hi-z)
Digitization: having problems w/ Wilkinson ADC

Some bits appear to still be counting once counter is stopped – leakage may be cause after several microseconds of storage (currently doing simulations)
Summary

working: timing, sampling, readout, ramp
not working: A/D
not tested: internal trigger

Plans

Confirm A/D problems. If leakage is culprit, should be able to accurately digitize readout cells within a few microsecs.

Possibly design a board with external ADC for use with Chan1 analog-out. This would allow for further chip characterization.
Sampling speed measurement:

Using sine wave input to chan1, used the analog out option to measure the sampling rate (topping out ~11 GS/s)
Sampled waveforms using Analog-out

1.25 GS/s

11 GS/s

Notes: Analog values are stored on buffer input capacitance, not designated sampling capacitor. (due to error in schematic)

Noise seen here dominated by set-up (scope, probe, etc.). We are currently designing board with external ADC to better characterize the noise/bandwidth