Design Review

PSEC3 8-2-2010

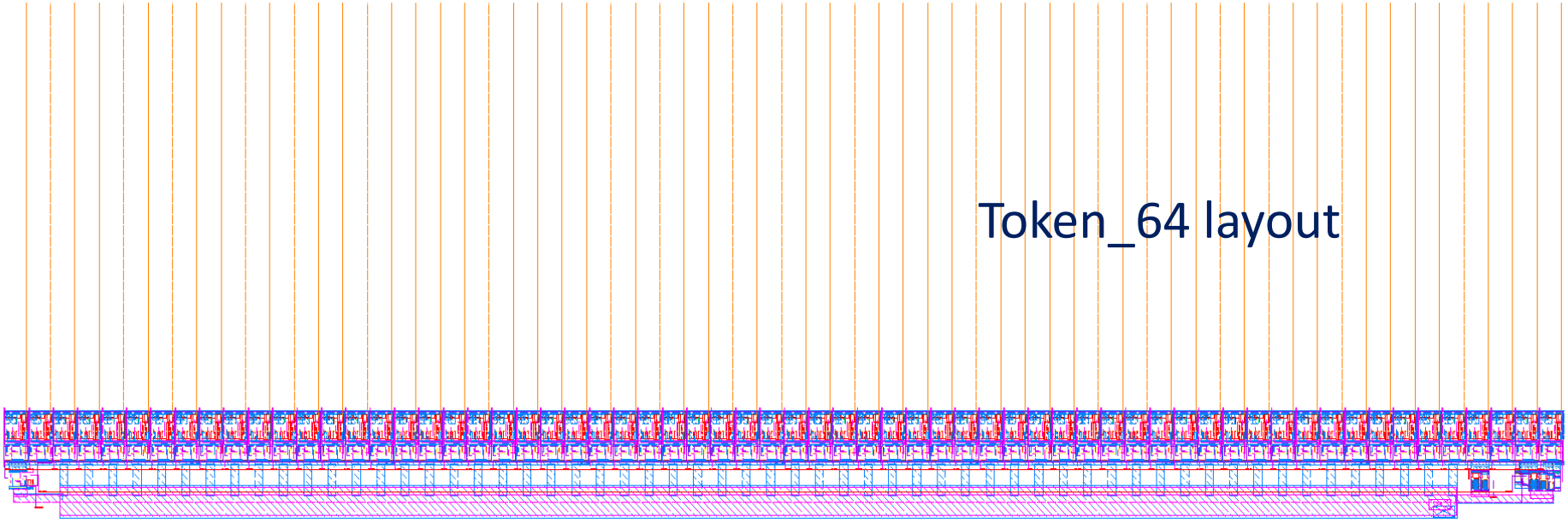
Readout

- structure
- target specs

Eric Oberla

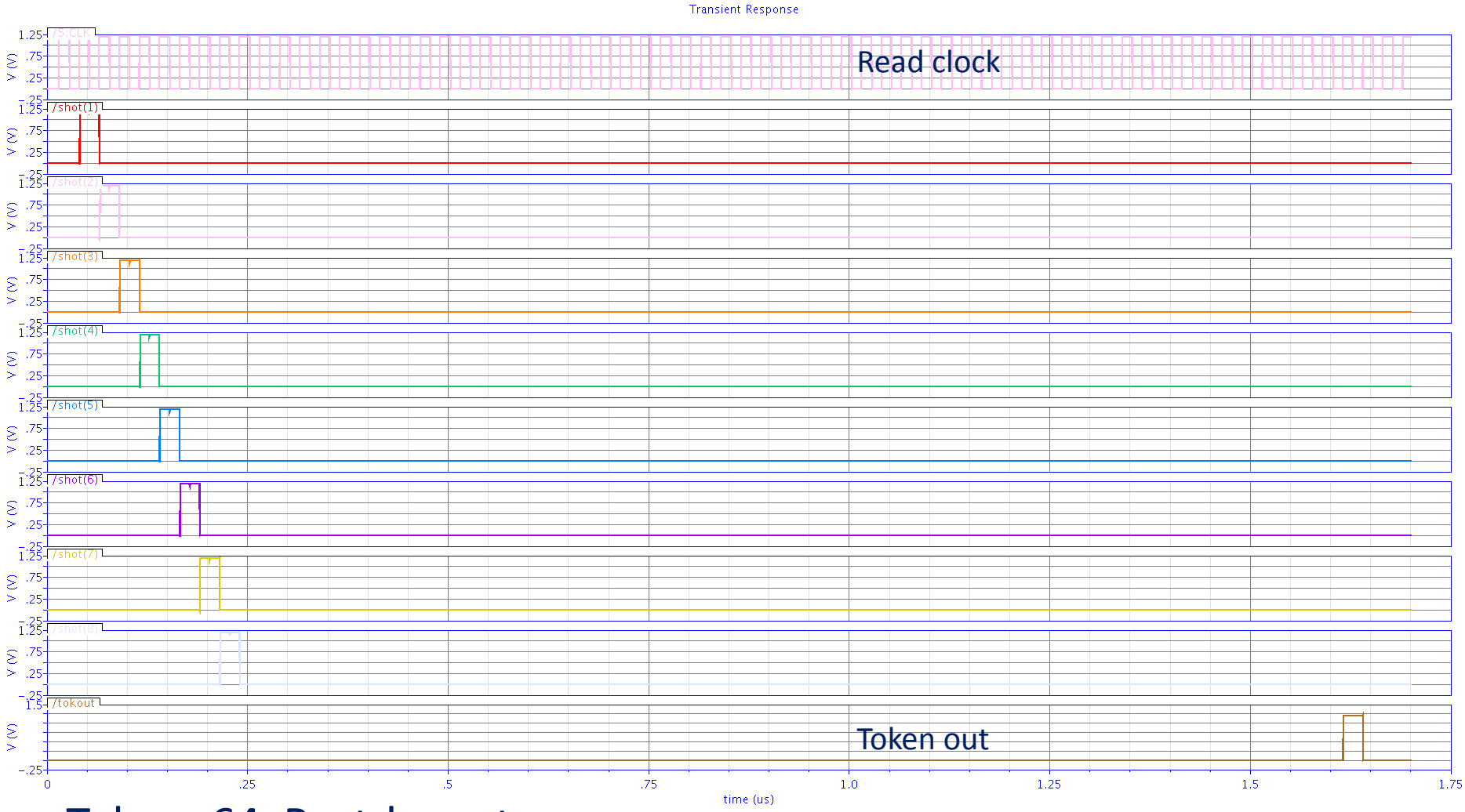
Token readout

- Shift register with one-shot logic
- Same design as on PSEC2 (worked as expected)



- Token made up of 4 Tok_64 blocks
- Readout blocks of 64 cells: 1-64 65-128 129-192 193-256
- Address data with Channel_select and Token_block_select + Read_Clock

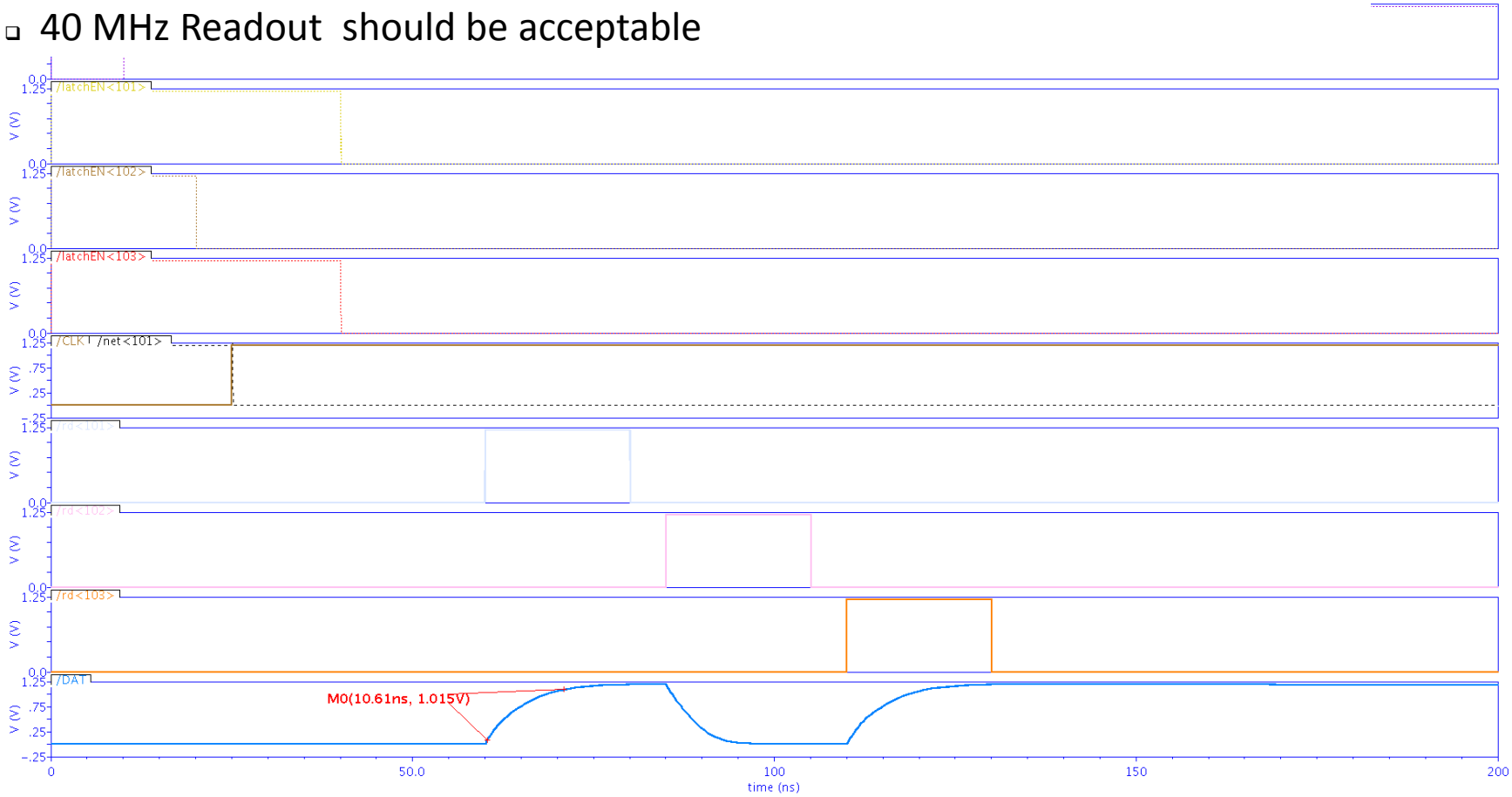
simulation



Token_64 Post-layout

Data bus settling time

- Data bus capacitance = 505 fF from post-layout extraction, settling time~10 ns
- Simulation using 256 cells tied to common bus
- 40 MHz Readout should be acceptable

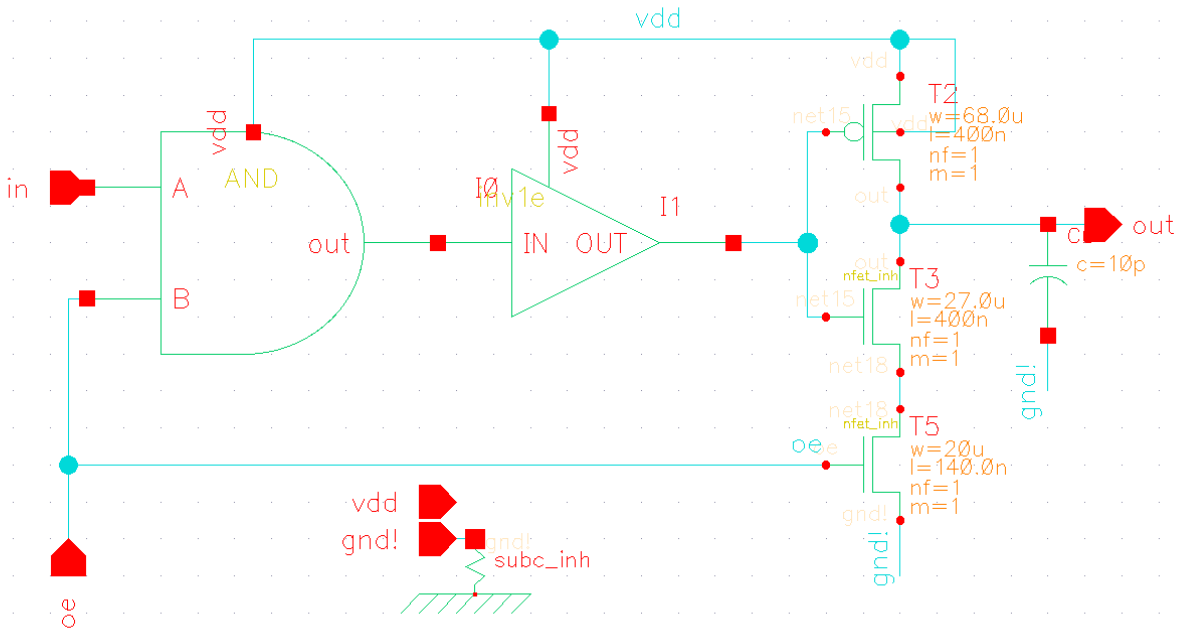


- This goes to another driver before the chip-wide data-bus

Tri-state pad driver

- When outfitting detector, we will likely tie data buses of several chips together

-> need tri-state pad driver with ‘chip_select’ bit



- Layout not completed... was waiting to get access to CERN pad library, but no luck yet. Anyway, simulations look OK(see next slide)

Tri-state pad driver - simulation

10 pF load -> ~2.3 ns rise/fall time