Design Review

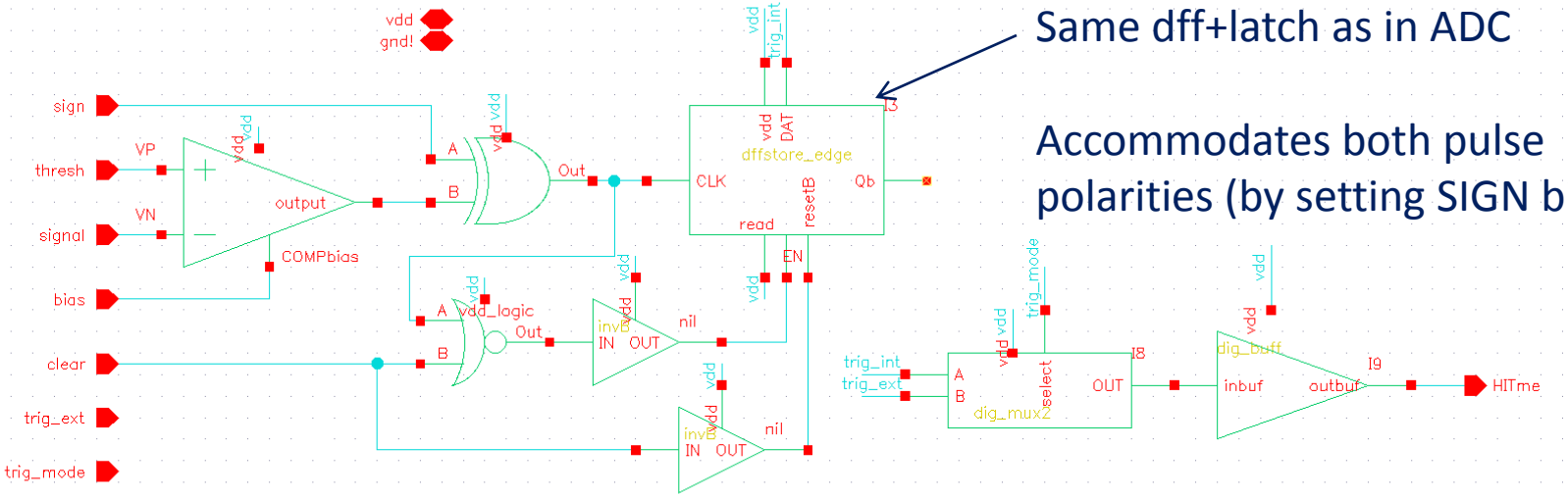
PSEC3 8-2-2010

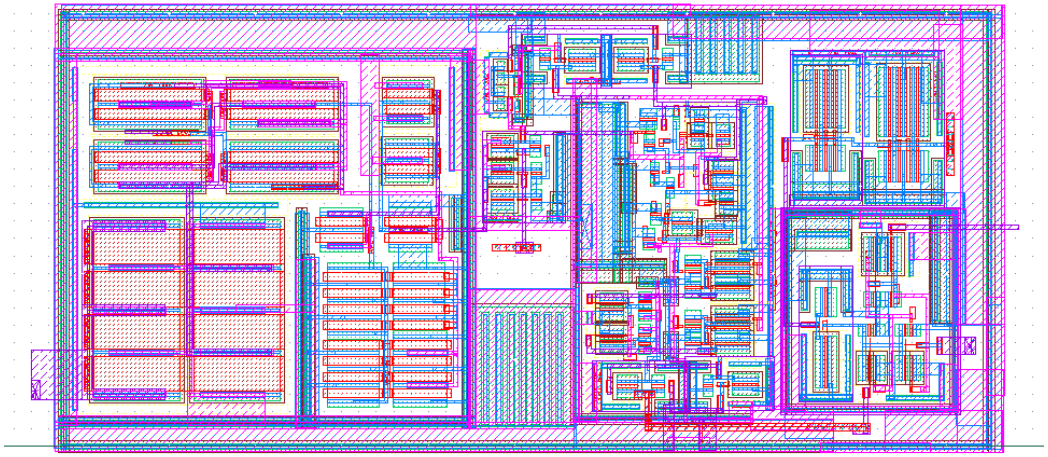
Trigger

- structure
- triggering scheme

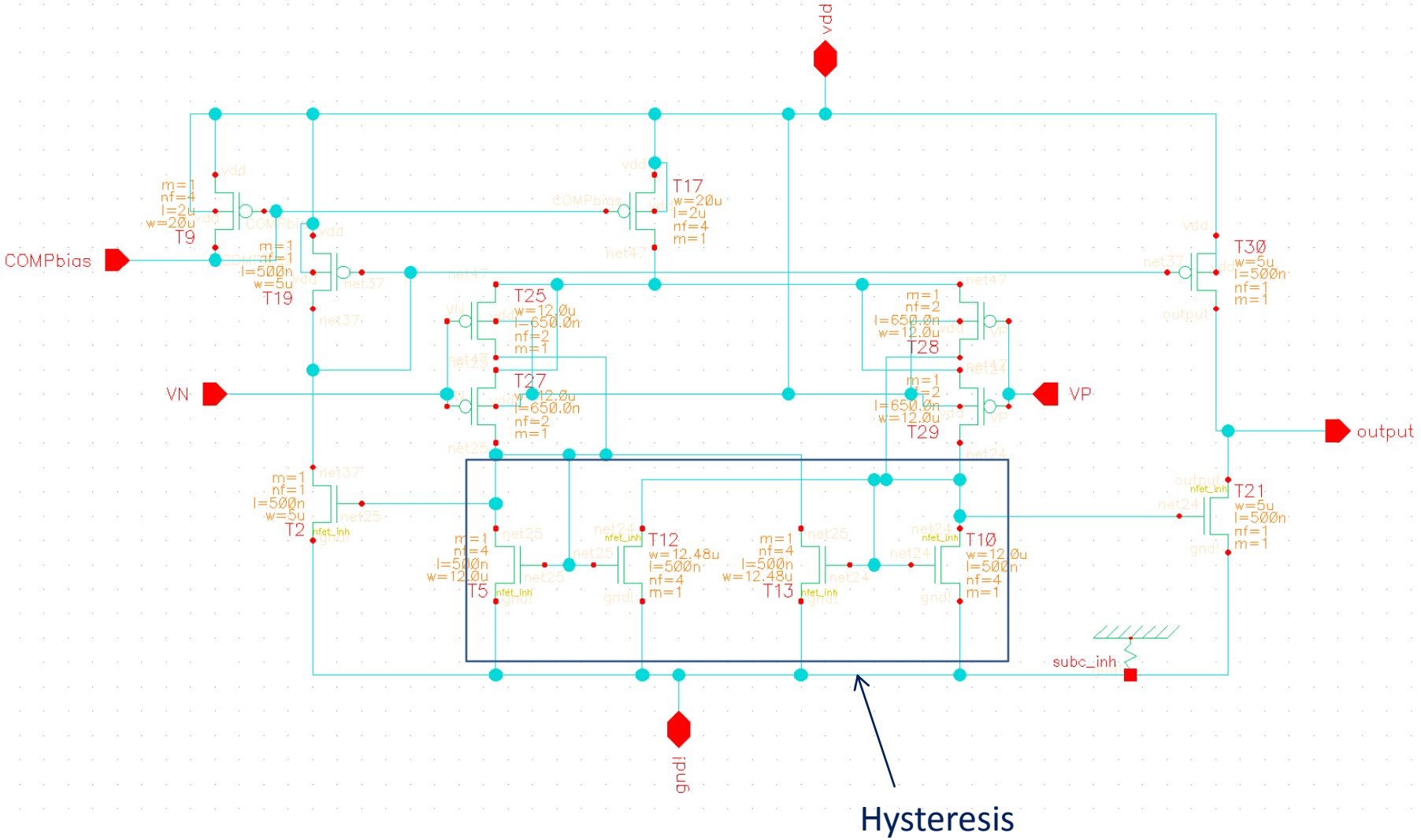
Eric Oberla

schematic/layout



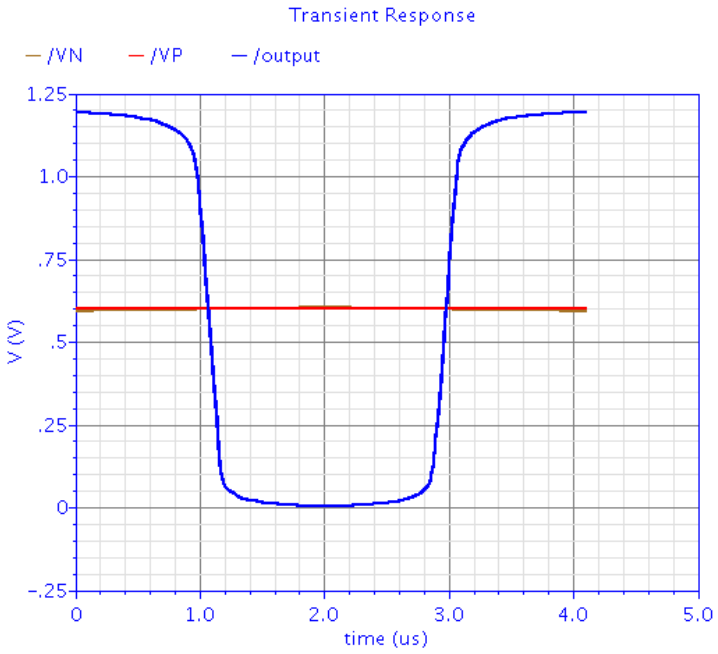


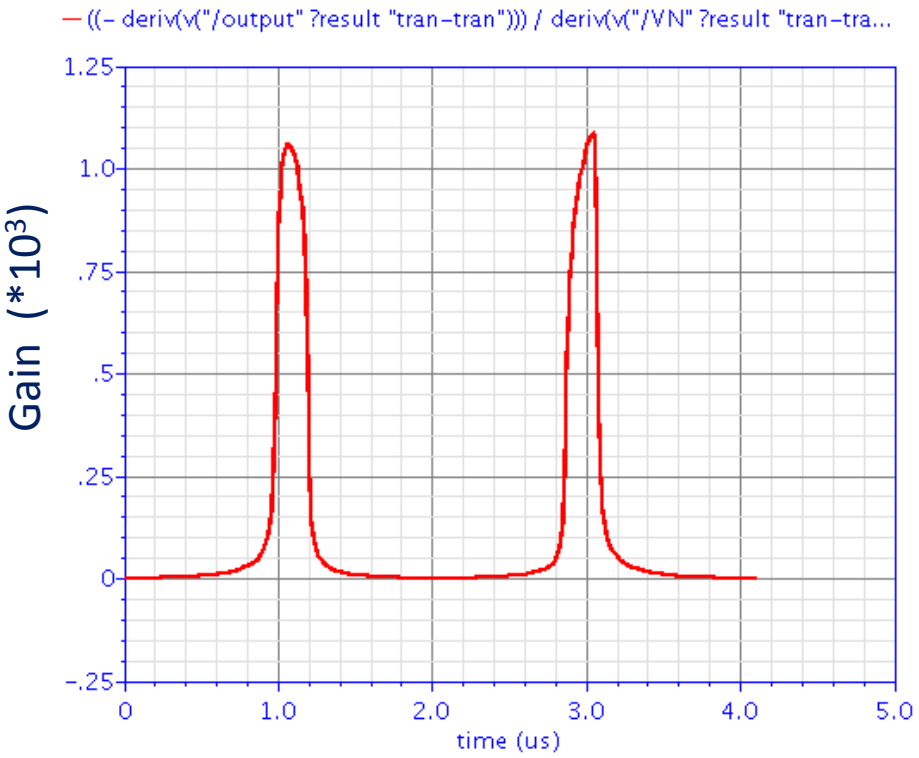
comparator


vdd
COMPbias
VN
VP
output
gnd!
subc_inh
T9
T17
T19
T30
T25
T27
T28
T29
T2
T12
T5
T13
T10
T21
Hysteresis

comparator

Gain = 1000 (nearly independent of bias 20-100 uA)





Triggering scheme

- Each analog input discriminator has a dedicated output pad

- There is also a triggerOR output. This is the OR of the five trigger signals.
  - This will be useful when outfitting an 80 channel detector, reducing the number of traces by a factor of 5 (if we only care about trigger/chip rather than trigger/channel).

- Individual trigger and/or triggerOR output(s) sent to FPGA, which resends common trigger that freezes all channels. This must be done within 25 ns, before sampling cells are overwritten.

- Channel 6 is a dedicated timing channel, allowing location of triggered event

- Readout all channels, or only those of interest

simulation (post-layout)