Design Review

PSEC3  8-2-2010

Trigger
  - structure
  - triggering scheme

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Same dff+latch as in ADC
Accommodates both pulse polarities (by setting SIGN bit)
comparator

Hysteresis
comparator

Gain = 1000  (nearly independent of bias 20-100 uA)
## Triggering scheme

- Each analog input discriminator has a dedicated output pad

- There is also a triggerOR output. This is the OR of the five trigger signals.
  - This will be useful when outfitting an 80 channel detector, reducing the number of traces by a factor of 5 (if we only care about trigger/chip rather than trigger/channel).

- Individual trigger and/or triggerOR output(s) sent to FPGA, which resends common trigger that freezes all channels. This must be done within 25 ns, before sampling cells are overwritten.

- Channel 6 is a dedicated timing channel, allowing location of triggered event

- Readout all channels, or only those of interest
simulation (post-layout)