Design Architect® Board Station® XE to DxDesigner® Expedition®
Stand Alone Translation Guide

Software Version EE7.9
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Design Architect/Board Station XE

To

DxDesigner/Expedition

“Stand Alone” Translation Guide

Translator Version: EE7.9
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Introduction

The DAD7.9 translator includes a DA to DxDesigner schematic translator and a Board Station to Expedition translator. Each can be used independently. This document describes the recommended process for translating a schematic and board and integrating the two.

Translation Process:

Synchronization Process:

When the words “Play Now” appear beside a section title, that section of the document has a corresponding e-Learning video. These videos have been provided at the following location:

http://supportnet.mentor.com/reference/other-info/Migrate-DA-BS-to-DxD-EE.cfm
1 Software Requirements

The following are requirements and recommendations as to the software that needs to be loaded on the computer to complete the conversion process. Other software may be required outside the recommended software below.

Mentor Graphics Software:

- Expedition Enterprise 7.9
  - DxDesigner
  - CES
  - Expedition
  - Library Manager
  - Translators (from standard install tree)
    - Layout and Library Translators
    - Schematic Translators

- Board Station XE 2007.7
  - MWE Runtime
  - Design Architect
  - Board Architect
  - CES for the XE Flow
  - Board Station XE
  - Falcon Framework
  - Librarian
  - PCB Package

Other software required:

- ActiveState Perl

Scripts referred to in this document:

- BrokeBackTraces.efm (Automation Script) [http://communities.mentor.com/mgcx/docs/DOC-1933](http://communities.mentor.com/mgcx/docs/DOC-1933)
- Connectivity Check Script (Automation Script) [http://communities.mentor.com/mgcx/docs/DOC-1820](http://communities.mentor.com/mgcx/docs/DOC-1820)

Visit the Automation Community for other helpful scripts: [http://communities.mentor.com/mgcx/community/pcb/design_tasks/migration](http://communities.mentor.com/mgcx/community/pcb/design_tasks/migration)
Software Requirements (Continued)

License(s) needed for Translation:

The translators are not licensed, but do require the following product licenses during translation.

DA2DX translator product license requirements:
- falconlib
- viewdraw
- designdataport
- encryptdecrypt

BS2EXP translator product license requirements:
- pcblibrarian
- falconprereq
- falconlib
2 DA\BS Design Preparation

Before the Design Architect (DA)/Board Station (BS) design can go through the translation process, some pre-translation steps are required to ensure the best translation possible. A utility (BS2EE Design Update) was created to help streamline the pre-translation step process. The utility will help to clean up the viewpoint, update the schematic based on DxDesigner translation requirements such as removing piped part numbers, build the design in Package, create or update CES from Layout, and create or update BSRE from Layout.

2.1 Check References (Optional)  

Running Check References is optional but recommended to ensure all paths are relative to the design.

2.1.1 Open DMGR

2.1.2 Browse to the design directory (In this example: C:/Demonstrations/BSXE_sdd_demo/SystemDesign)

2.1.1 Select the design folder

2.1.2 Open Check References (Edit ► Check References)

2.1.3 Set “Traverse References” to Traverse

2.1.4 Select the Options button
2.1.5 Set Broken Reference Limit to 5000

2.1.6 Select OK to close the options window

2.1.7 Select OK from the base dialog

2.1.8 Change the paths to conform to where the design is currently located:
   •  SSDD_DEMO → C:/Demonstrations/BSXE_sdd_demo/

   Note: The From/To is case sensitive and requires forward slash “/” and not back a back slash “\”.

2.1.9 Set “Change pattern occurrences” to Every

After the process has completed, the following message will be displayed:

2.1.10 Select “Yes” to run another check. This need is because the path provided still might be wrong or there were more than 5000 broken references. Continue to run Check References until the process says, “No broken references were found” in the status block.

End “Check Reference” Video
2.2 Modify Cell_Type Attribute

To prevent merging of nested geometries, the CELL_TYPE attribute must be added to generic geometries in the library.

For more information, please refer to the Configuration Guide.

2.3 Remove Locking Files

Remove any files in the “CDA folder” in the Board Station PCB directory. Files found here are locking file, and failing to remove these files will result in a translation error.

2.4 Remapping User Layer Reference Designators

In the BSXE to Expedition translation there is no additional method of mapping layer data. The design is already in the BSXE/Expedition layer structure. The only difference between BSXE and Expedition is that BSXE allows reference designators to be on a User Layer and this is not allowed in Expedition.

NOTE: If your design has Reference Designators on User Draft Layers, you will need to modify them to be on the Assembly_Reference layer or Silkscreen_Reference layer. Expedition does not allow a Reference Designator to be on a user layer. If you do not modify this situation the Reference Designator will be translated as dumb text. If this situation exists on your design, follow this additional process prior to translating the design into Expedition.

For User Layer Reference Designators that need to map to the Silkscreen layer, set the Environment Variable “MGC_RETAIN_DEL_REF” = <User Layer name”. This will stop BSXE from adding back into the design Reference Designators that have been deleted from the user layer.

2.4.1 Open the design in Librarian.

2.4.2 Using the Geometries pull down menu, select Open Geometries.

2.4.3 Set the Geometry filter to be Components.

2.4.4 Select the Open All selection and OK the Geometry dialog window.

2.4.5 In one of the geometries, using the Setup pull down menu select Edit Layer.
2.4.6 Select the SILKSCREEN or <<the layer that ASSEMBLY_OUTLINE is mapped to in the BSXE_data_mapping.ini file>> selection.

2.4.7 Select the TEXT icon window setting.

2.4.8 Select Reference Designator and select the CHANGE LAYER icon.

2.4.9 Select OK in the popup window to move the text to the layer selected as the Edit Layer.

2.4.10 Repeat this process for every Component Geometry.

2.4.11 File SAVE and EXIT out of Librarian.

2.4.12 Open the design in BSXE.

2.4.13 Using the Setup pull down menu select Project Integration.

2.4.14 Set the Library Extraction Option to be "Update Local Libraries with newer Geometry data".

2.4.15 Select the Green light next to the "No Connectivity to be Forward Annotated" selection to run Forward Annotation.

2.4.16 Close the Project Integration window.

2.4.17 Using the ECO pull down menu, select Replace Cell.

2.4.18 Select RESET in the Process Type setting.

2.4.19 Toggle on every cell in the list.

2.4.20 Make sure the "Keep Text Attributes During Replace" setting is toggled on.

2.4.21 Select the OK button in the Replace Cell window.

2.4.22 Review the moved Reference Designators on the Assembly Items, REF DES TOP and REF DES BOTTOM layers located on the PART tab of Display Control.

2.4.23 Correct any rotation or placement issues by comparing it to the user layer that the Reference Designators were on previously.

2.4.24 File SAVE and EXIT out of BSXE.
2.5 **BS2EE Design Update Setup**

A few steps are required before the BS2EE Design Update Utility will work for the first time.

**NOTE:** The following steps require access to the Microsoft Windows Environment Variables. If the current user does not have write access the Environment Variables, please contact the IT department for assistance.

- **2.5.1** Extract the BS2EE Design Update Utility (downloaded from Mentor Community). Remember where this package is extracted to, the path will be needed in the next step.

- **2.5.2** Open Environment Variables (Start ► Control Panel ► System ► Advanced ► Environment Variables)

- **2.5.3** Create a new System Variable called “BS2EE_TK” with a variable value of where the utility was extracted to in step 2.2.1.

![Edit System Variable](image)

Now that the system variable has been created, it needs to be added to the ample path.

- **2.5.4** Add “$BS2EE_TK” to the AMPLE_PATH system variable

![Edit System Variable](image)

- **2.5.1** Exit Environment Variables
Now that the utility has been set up in the environment variables, it will be recognized in DMGR, DA and BA. This utility can add lines with Net Names to pins that just have a net name assigned to the pin, add INST names to unnamed blocks, enable CES, remove pipes from Piped Part Numbers and ensure the schematic and board are in sync.

2.6.1 If DMGR is not open, open DMGR

2.6.2 Select the Design Container

2.6.3 Select the BS2EE Design Update Utility from the new BS2EE pull down menu

2.6.4 Select “Yes” for the following option(s):

- “Remove un-used viewpoint references” - Clear viewpoint references that are no longer used in the design.
- “Remove annotation issues from pcb vpt” – Removes back annotation data from the viewpoint that can cause problems. This removes the annotation “PART_NO <annot_deleted>” from the viewpoint if such annotations exist.
- “Update schematic sheets for translation”
Under “Update schematic sheets for translation”, select the boxes:

- “Add net names” – Adds default nets defined by function
- “Add net lines” – Adds net names to pins with netname assignments defined by function assign_netnames
- “Add INST names” – Adds instance names to default named hierarchal blocks defined by function assign_instnames().
- “Add PN_NOPipe” – The command adds a new property “PN_NOPipe” to each symbol, with a value matching the PART_NO property with the piped suffix removed.

2.6.5 **Optional:** Select “Yes” for the following options:

- Package design after schematic updates
- Synchronize layout data after schematic updates

2.6.6 Click “OK” to execute the options on the schematic.

2.6.7 After the Update Utility has completed, close DMGR.

*End “BS2EE Design Update Utility” Video*
3 Translation of the Board Station PCB to Expedition PCB

3.1 BS2EXP Geometry Layer Configuration

BSXE uses the BSXE_data_mapping.ini file to map Board Station layers to BSXE layers.

If any layer modifications are required, please refer to the Configuration Guide.

3.2 Layer_File Configuration

The Board Station to Expedition translator requires access to the design’s layer_file.

Copy design’s layer_file to the BSXE install tree:

- \MGC_HOME.ixz\pkgs\pcb_base\data
- \MGC_HOME.ixz\pkgs\pcbxe_base\data

3.3 Translation of the Board Station PCB to Expedition PCB

Now that the translator template files have been modified, the following steps will take the Board Station PCB data and translate it into Expedition PCB data. The first step to translating a Board Station PCB design is to configure the Mentor Graphics tools for the EE7.9 Flow.

3.3.1 Run the Configurator to advance to the Expedition Enterprise 7.9 flow (Start ► Programs ► Mentor Graphics SDD ► The MGC SDD Configurator)

3.3.2 Open the BS2EXP Translator Shell (Start ► Programs ► Mentor Graphics SDD ► Translators ► BS2EXP Translator)
3.3.3 Open the BS2EXP Translation Wizard (Translate ► BS2EXP Wizard)

![BS2EXP Translation Wizard](image)

3.3.4 Choose the Source Design

3.3.5 Choose the Target location. It is recommended in adding Exp_ to the folder name to distinguish that this the translated Expedition design.

3.3.6 Set the Output Unit to “Obtain from Design”

3.3.7 Ensure that the following have been enabled:

- Preliminary Step
  - Initialization target directory
  - Create seed
  - Save geoms
  - Prepare design
- Intermediate step
  - Prepare XE data
  - Create netlist
  - Prepare XE cell data
  - Create PDB
- Import step
  - Import data to EE PCB
- Post Translation Steps
  - Open Design
  - Forward Annotate
  - Save and Close Design

3.3.8 Click “Run” to run the Translation Wizard Once the translator is running, the original Translator console window will update with more information as to what the translator is doing. When finished, the Expedition design will be located in the folder created earlier. At this point, the BS2EXP Translator has created a stand-alone, netlist driven, PCB design.

*End “Translation of the Board Station PCB to Expedition PCB” Video*

Note: After the translation has finished, now is a good time to create a zipped up copy of the results as a backup.
3.4 Moving the Central Library

After the Board Station translation has finished, it is recommended to move the central library created in the Expedition PCB folder to a more central location to the project.

This central library should be a building pointing for a corporate central library.
4 Design Architect to DxDesigner Schematic Translation

4.1 DA2DX Translator Configuration

The delivered translator configuration files are located at:
<path_to_install_target>\SDD_HOME\translators\win32\config\n
Review and, if needed, modify the schematic translation options in the da2dx.cfg file. An example of modification is scaling the DA schematic.

[DESIGN SCALING]
Scale=0.2 (this creates .2 pin spacing on a symbol)

If the DA design had Piped Part Numbers removed (as described in section 2.3), the following changes need to be made under [COMPONENT ATTRIBUTES] and [PACKAGE ATTRIBUTES]:

PART_NO=Piped Part Number
PN_NOPIPE=Part Number

NOTE: This is the only version of the da2dx.cfg file. Before making any changes, please make a backup copy. In the picture above, a .bak version was created as a backup.

4.2 Translation of Design Architect to DxDesigner

Now that the translator configuration files have been modified, the following steps will take the Design Architect schematic and translate it into DxDesigner schematic.

4.2.1 Create a folder to store the translated Schematic. This folder will become the parent folder for the whole project

4.2.2 Open the DA2DX translator (Start ► Programs ► Mentor Graphics SDD ► Translators ► DA2DX Translator)
4.2.3 For the “DA Design Directory,” click the “… ” to browse to the schematic folder

4.2.4 For the “DA Component (Schematic/Viewpoint)”, select the “pcb_design_vpt”

4.2.5 For the “Target Directory”, click the “… ” to browse to the parent folder created in step 4.3.1

Note: Do NOT choose the translated Expedition PCB folder created in step 3.3.5. The separation is required for a later step.

4.2.6 Check “Import Additional symbols to Design Specific Central Library”, and click the “…” to browse to the Central Library.lmc file located in the Expedition PCB folder.

4.2.7 Check “Generate PDB into Design Specific Central Library”

4.2.8 Uncheck “Normalize Symbols” – Leaving this checked would move the symbol origin to the lower-left corner of the symbol. This option should be used only when using an existing library where symbols have been normalized.

4.2.9 Leave “Normalize Design” checked – Much like the “Normalize Symbols” this places the schematic sheet origin at the bottom left of the schematic sheet.

Once completed, the dialog should appear much like the reference picture below.
DA2DX Translator Setting Reference

4.2.10 Click “Translate” to translate the schematic.

Translator Log Window:
Design Architect to DxDesigner Schematic Translation is Successful

*Completed DA to DxDesigner Schematic Translation:*

*EndTime:*

*Error(s): 0   Warning(s): 1*

*End “Translation of Design Architect to DxDesigner” Video*

At this point, the Design Architect to DxDesigner translation is complete. The next section will focus on post process steps such as adding Supply Rename to signals that the ALIAS POWER once covered, packaging the DxDesigner schematic and then forward annotating the DxDesigner information to the PCB template created earlier.
5 DxDesigner/Expedition Post-Translation Steps

5.1 DxDesigner Diagnostics

After a translation, it is recommended to run DxDesigner Diagnostics. DxDesigner Diagnostics helps to find and correct database inconsistencies stemming from unexpected events during the translation process.

5.1.1 Open DxDesigner (Start ► Programs ► Mentor Graphics SDD ► Design Entry ► DxDesigner)

5.1.2 Open the DxDesigner Schematic (File ► Open ► Project…)

5.1.3 Browse to the .prj file (in this case “SystemDesign.prj”) and click “Open”

5.1.4 After the project has opened, open the main block of the schematic (in this case “SystemDesign”)

Design Architect\Board Station XE to DxDesigner\Expedition Translation
5.1.5 Run DxDesigner Diagnostics (Tools ➤ DxDesigner Diagnostics)

5.1.6 Review log window for any errors or warnings.

End “DxDesigner Diagnostics” Video
5.2 Handling Global Net Overrides (Optional)

In the Design Architect/Board Station flow, the ALIAS_POWER attribute in the pkgconf.pkconf file allows for the global rename of signals. DxDesigner/Expedition does not have the same capability of a global signal rename; instead DxDesigner uses “Supply Rename” to rename implicit signal pins to a different net. To get a list of all parts that need the “Supply Rename” attribute added, a program needs to be run:

5.2.1 Open DA2DX Supply Rename (downloaded from Mentor Community)

![DA2DX Supply Rename](image)

5.2.2 Browse to the parent folder of the DA/BS Design

If the DA/BS Design does not contain any Power Alias information, the following window message will be displayed:

![DA2DX Supply Rename](image)

5.2.3 Browse to the parent folder that contains the Map Files for this project

5.2.4 Browse to the DxDesigner .prj file created during the DA2DX translation.

5.2.5 Press “Process” to compile a list of part numbers that need the “Supply Rename” attribute added.

To produce a log file after processing:

5.2.6 Click back to the Design Info window

5.2.7 Click “Export”

5.2.8 Browse to a text file to export the information to and click “Open”
5.3 Adding Supply Rename to Schematic (Required using Section 5.2)

Now that the script has supplied the Supply Rename recommendations, it is time to apply those recommendations to the schematic.

5.3.1 Open the log file created by the DA2DX Supply Rename program.

Example:

Symbol Property:
SUPPLY RENAME

Property Value to add to symbol in schematic:
AGND=GND

Part Numbers to add symbol property and value:
V4FX100

5.3.2 With the DxDesigner project open, open the “Find and Replace Text” dialog (Edit ➤ Find/Replace…)

5.3.1 Click “Find All” to find all parts in the schematic (in this example “V4FX100”)

The output window gives results that are linked. Click on the arrow beside the result to find that part in the schematic.
5.3.2 If the “Supply Rename” attribute is not available in the property window, add the property “Supply Rename” and add the Property Value from the Supply Rename log.

5.3.3 Repeat this process for all part numbers in the Supply Rename log.
5.4 Renaming Global Signals in DxDesigner (Required using Section 5.2)

After adding the Supply Rename attributes to the recommended part numbers, there still may be global signals that need to be renamed.

Open the project in DxDesigner and execute the steps of either the automated method or the manual method to modify the global signals.

Automated Method:
Although the automated method is the fastest way to search through a project and replace text, it is not always guaranteed to find all items. Even when it does find all items, it is not guaranteed to replace all items with the new text.

5.4.1 Open the “List Global Signals” applet (Tools ► List Global Signals)
5.4.2 Open Find and Replace applet (Edit ► Find and Replace)

End “Global Net Overrides” Video
Manual Method

5.4.3 Open the “List Global Signals” applet (Tools ► List Global Signals)

This window will reveal every global signal, page by page, used in the design.

In the following steps, “AGND” will be renamed to “GND”.

5.4.4 Click on the arrow beside the global signal to advance to that page and select the global signal symbols.

5.4.5 With the global symbol selected, look at the properties window.
5.4.6 Rename “AGND” to “GND”

5.4.7 Repeat this process for all Global Signals that need to be renamed.
6  DxDesigner/Expedition Synchronization

In the following sections, synchronization between the translated schematic data and translated PCB data will happen. With the post translation steps now complete, the first step will be to package the schematic data in preparation of synchronization with the previously translated PCB data. After packaging, it will be time to associate the PCB template file created in section 4.1, followed by pushing the schematic data package into Expedition. Finally, the data in Expedition will need to be reviewed.

6.1 Packaging DxDesigner

This is part of a normal DxDesigner / Expedition design process. This step will assign PDB part numbers (from the library) to the symbols and check for any errors in the schematic.

6.1.1 Open the Packager applet (Tools ► Package…)

6.1.2 Enable “Allow Alpha-Only Reference Designators”

6.1.3 Select “Rebuild Local library data; Preserve locally built data”

6.1.4 Select “OK” to package

A successful schematic package will end with the following in the output window:

*The Common Database has been successfully updated.*
-Packager finished successfully.*
-*!THE iCDB IS UP-TO-DATE!*
6.2 Debugging Packager Errors

Sometimes packager will not complete successfully. The following is only guidance and is not a complete list of packager errors and solutions. Please refer to SupportNet for more information on errors not described here.

6.2.1 Missing Part Number

- **There is no Part Number: <###> in the Parts DataBase for symbols with Part Name: (null) and Part Label: (null). Please add the Part Number to the PDB either directly or by having the project file point to a PDB that contains it.**

The "There is no Part Number" error means either the Part Number defined on the symbol does not exist in the Central Library or the Part Name and/or Part Label on the schematic symbol do not match the Part Name or Part Label defined in the PDB for that Part Number. To remedy the problem, do one of the following:

1. Replace the device on the schematic using Component Replace.
2. Edit the properties on the schematic symbol to match the Part definition.
3. Edit the Part definition to match the schematic symbol properties.
4. Delete the symbol/device from the schematic and then Place Device again.

If the Part Numbers in question are known to exist in the Central Library and Name/Label match, then the PDB partitions that contain the Part Numbers may not be available to the Packager. To fix this, do the following.

1. Open the Central Library in Library Manager
2. Select Setup>Partition Search Paths from the menus
3. Select the scheme from list
4. Click the PDBs tab and toggle on the appropriate partitions
5. Click OK to save. Close Library Manager
6. Package the schematic design (or forward annotated) again

6.2.2 Pin/Port Mismatches during Hierarchy

*Error on block <block_name>, pin <pin_name> on block <block_id>: Pin/Port name mismatch between parent block and child schematic. This pin not found in child block.*

Or

*Error on block <block_name>, symbol <symbol_name>: Pin name mismatch between parent block and child schematic. Child schematic has more pins.*

Packager first checks that ports on the hierarchical block have corresponding Pin Type connectors in the lower-level schematic. Then it compares the width of bus connections that traverse the hierarchy ensuring that the port at the Block interface matches the corresponding pin in the lower level schematic.
6.3 **DxDesigner/Expedition CES Synchronization**

With the schematic successfully packaged, CES rules need to be synched between the translated schematic and the translated PCB before the first forward annotation can occur. A program was created to export CES data and stack-up information from Expedition PCB and import the data to DxDesigner. During this process, the program reconciles any differences between net names and stack-up information found in DxDesigner and in Expedition.

6.3.1 Open SynchBSMigratedDesigns.exe (downloaded from Mentor Community)

6.3.2 Click “…” to browse to the schematic’s .prj file

6.3.3 Click “…” to browse to the PCB .pcb file created during the board translation.

6.3.4 Enable “Import PCB Constraints to Schematic”

6.3.5 Press “OK” to execute the program.

When the script has finished the dialog window closes.

*End “CES Synchronization” Video*

6.4 **Project Association and Opening Expedition PCB**

With the schematic successfully packaged and the CES data now in synch, it is time to associate the translated PCB with the translated schematic.

6.4.1 In an Explorer window, browse to the translated Expedition PCB folder

6.4.2 Copy the PCB folder from the translated Expedition PCB parent folder into DxDesigner Schematic parent folder.

Example:
- Translated Expedition PCB (Parent folder):
  C:\demonstrations\BSXE_sdd_demo\Exp_SystemDesign\n- Translated DxDesigner Schematic (Parent folder):
  C:\demonstrations\BSXE_sdd_demo\DxD_SystemDesign\
Copy PCB from Expedition PCB folder:
C:\demonstrations\BSXE_sdd_demo\Exp_SystemDesign\PCB

- Into DxDesigner Schematic folder:
  C:\demonstrations\BSXE_sdd_demo\DxD_SystemDesign\PCB

6.4.1 Open Expedition PCB (Start ➤ Programs ➤ Mentor Graphics SDD ➤ Layout ➤ Expedition PCB)

6.4.2 Open the Expedition PCB file (File ➤ Open) copied to the DxDesigner schematic folder from step 6.4.2
6.4.3 Browse to the .pcb file in the schematic PCB folder and click “Open”

Since the PCB was copied to a new location, the reference to the project file has been lost:

6.4.4 Click “Yes” to and browse to the DxDesigner project file.

DxDesigner has newer data than Expedition. That information needs to be transferred forward into expedition. The following should appear:

6.4.5 Click “Ok”

6.4.6 Click “Yes” to proceed with Forward Annotation.

6.4.1 Click “Yes” to bring up Project Integration or “No” to wait to proceed with Forward Annotation at a later time.

End “Expedition PCB Association” Video
6.5 Project Integration and Forward Annotation

Project Integration is used to establish a link between the DxDesigner schematic, CES and Expedition PCB. It also designates how the flow of information between DxDesigner/CES/Expedition is to be handled either through Back Annotation or through Forward Annotation.

6.5.6

6.5.1 Change Unused Parts from “Change to Spares” to “Delete”

6.5.2 Under Library extraction options, select “Rebuild local library data; preserve locally built data”

6.5.3 Unselect “Remove floating traces & Vias”

6.5.4 Unselect “Remove hangers”

6.5.5 Select “Assign single pin nets to unused pins, enabling fanout”

6.5.6 Push the first amber button to forward annotate

A successful Forward Annotation will end with one of the following:

6.5.7 Review the Forward Annotation.txt file (File ➤ File Viewer)
7 Validation and Cleanup

Now that the design is synchronized (schematic and PCB), the design data needs to be reviewed for correctness and completeness in the following areas:

- Broken traces
- Open Fanouts and Netlines
- CES rules
- Verify Netlist Integrity
- Route Tiny Opens

7.1 Diagnosing “Broken Back” Traces

If the Forward Annotation log lists broken back traces, the schematic and board do not match in some way. To diagnose what is happening, the location of each broken back trace will be displayed in the forward annotation log in DBU units.

No matter what unit the design was created in, Expedition handles numbers in a generic DBU (DataBase Unit) and since the display units in Expedition cannot be set to DBU, an Automation script was created in helping to diagnose broken back trace problems.

7.1.1 From within Expedition, open BrokeBackTraces.efm (File ► Open Script Form) (downloaded from Mentor Community)

7.1.2 Browse to and select the script where it was saved locally

7.1.3 Click “Open”
7.1.4 Once the script is open, there are two options.

- **Auto Populate User Layer:** While reading the forward annotation list, the script will populate a user layer called “Broken Back Traces” with “X” where the center of the “X” is where the broken back trace is located.
- **Populate User Layer During Cross Probe:** Populates the user layer “Broken Back Traces” with only the coordinates double clicked.

7.1.5 Click “Report” to populate the list with locations of the broken traces

7.1.6 After the list has been populated, double clicking any coordinate will zoom into the area of the broken back trace.

*End “Diagnosing “Broken Back” Traces” Video*

### 7.2 Review Open Fanouts and Netlines

Review the Review Hazards dialog for opens. On occasion, there will be a plane that has had a net change (from /I3215/N41234, to N41234). This may cause the plane shape to become Net0 and thus unconnected from the pins. From within Expedition, open Review Hazards (Analysis ► Review Hazards)

7.2.1 Select “#” icon (bottom left hand corner) to update the Review Hazards dialog

7.2.2 Select Online

7.2.3 Review the Open Fanouts and the Open Netlines section for any hazards.

In the case that the net name associated to the plane shape has changed or been removed, the plane will need to be corrected manually.
7.3 **Review CES Rules**

It is important to review the CES data of the design. There are occasions where nets get improperly associated or un-associated to the constraint classes.

7.3.1 Expand the Net Classes and Constraint Classes sections in the Navigator and review the number of assigned to each.

7.3.2 Select the Nets tab and review the nets associated to each constraint class.

7.3.3 Review net ordering, topology assignment and pin pair assignments.

7.3.4 Exit CES and Save the Expedition Design.
7.4 Verify Netlist Integrity

Due to differences in net naming conventions between DA and DxDesigner, it is normal to see nets being renamed. A script was created to catch any differences in pin-to-pin connectivity, which would be indicative of errors in the translation process. The script looks at each pin on each net in the original Board Station net.nets file, and compares the net name that is connected to that pin in CES. Net renames and differing connectivity is reported.

7.4.1 Insure ConnectivityCheck.vbs is located in the WDIR folder (downloaded from Mentor Community)

7.4.2 From within DxDesigner, open CES (Tools ► Constraint Editor System (CES))

7.4.3 Run the script by keying in ConnectivityCheck.vbs in the Command Line toolbar (View ► Toolbar ► Command Line)

7.4.4 Provide a path to the PCB directory

After the script completes, the results are shown in the System tab of the CES Output window...

End “Verify Netlist Integrity” Traces” Video
7.5 Route Tiny Open Nets

Occasionally open netlines (very tiny open nets) appear after translating a design to Expedition. These are caused by cell replacement, where trace ends do not exactly match the pad center.

Display Control Dialog

7.5.1 Select display scheme Loc:All On from the Display Scheme pull-down.

7.5.2 Ensure the following options are checked:
- Ordered & Open Netlines
- All Open MST Netlines, Netlines From Traces (Netlines From Traces are particularly important: if not checked, routeTinyOpens.pl will not route those opens at all)

7.5.3 Ensure the following options are NOT checked:
- Ordered & Routed Netlines
- Classlines (Class lines are not important, but can be confusing if shown.)
Editor Control Dialog – Route tab/Plow

7.5.4 Ensure that the following option is NOT checked:
- Prevent loops

Editor Control Dialog – Route tab/Vias & Fanouts

7.5.5 Ensure that the following option is NOT checked:
- Enable fanout of single pin nets
Editor Control Dialog – Route tab/General Options

7.5.6 Ensure that the following options are NOT checked:

- Stub lengths
- Layer restrictions
- Via restrictions
- Max delays & lengths

Editor Control Dialog – Route tab/Dialogs/Pad Entry

7.5.7 Select the following:

- All Rectangular Pads
- Allow via under pad
- Allow off pad origin

This is to allow vias under pads for all rectangular pads (SMD) for boards that use this technique to fanout SMD pins.

7.5.8 Close the Editor Control Dialog
Fixing existing traces

All traces and vias should be set to “fix” before proceeding. This will minimize any undesired results from “glossing” operations while manual routes are attempted. It will also make it easier to see the results of routeTinyOpens.pl.

7.5.9 In Expedition, select Edit ► Select All

7.5.10 Select Edit ► Fix

Running routeTinyOpens.pl script

7.5.11 In Windows Explorer, browse to the location of the routeTinyOpens.pl script file and double-click to initiate the script (downloaded from Mentor Community).

7.5.12 A command window (DOS) will pop up, giving feedback on the task running. The “status” area (bottom of Expedition work area) in Expedition may also show progress. The script may run for several minutes on larger designs.

Update the design

The Expedition database must be reloaded after running the script because the Automation Layer does not perform a reload when the script is executed. None of the script changes will be shown until this reload has been performed.

7.5.13 Open Setup Parameters (Select Setup ► Setup Parameters)

7.5.14 Select the General tab
7.5.15 In the Test point settings area, select “Top” in the Test side drop down list, and then set it back to “Both”.

7.5.16 Select OK

The dialog closes, and the reloading of the layout database begins.

When control returns to the cursor, the changes in the current session have taken place. Nothing is filed permanently until a File > Save is performed.

End “Route Tiny Opens” Traces” Video