16-Channel, 14-Bit, 500 MHz ADC Module

The University of Chicago

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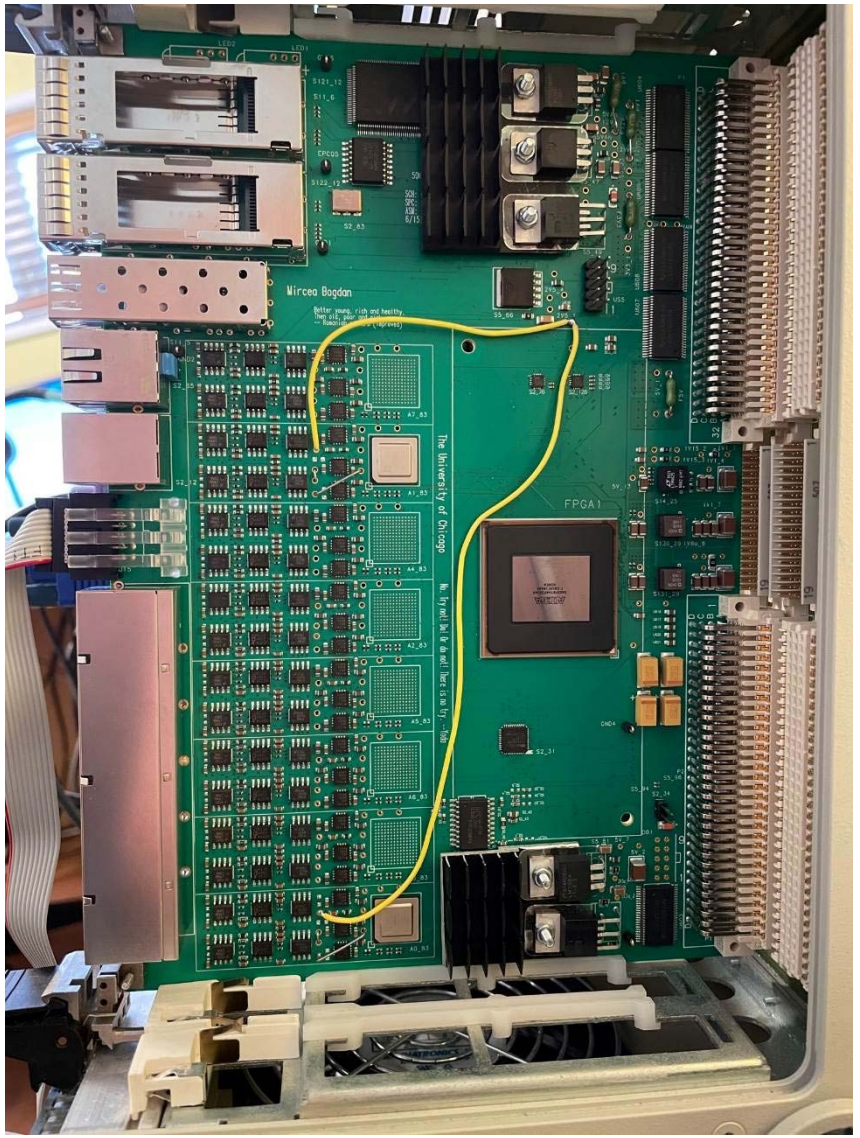
16-Channel,14-Bit, 500MHz ADC Board

Populated two Modules, received - 1/20/23

- One module with just two ADC chips
- One module with no ADC chips

Started testing



http://edg.uchicago.edu/~bogdan/14BIT_500MHz_ADC_Board/schematics.html

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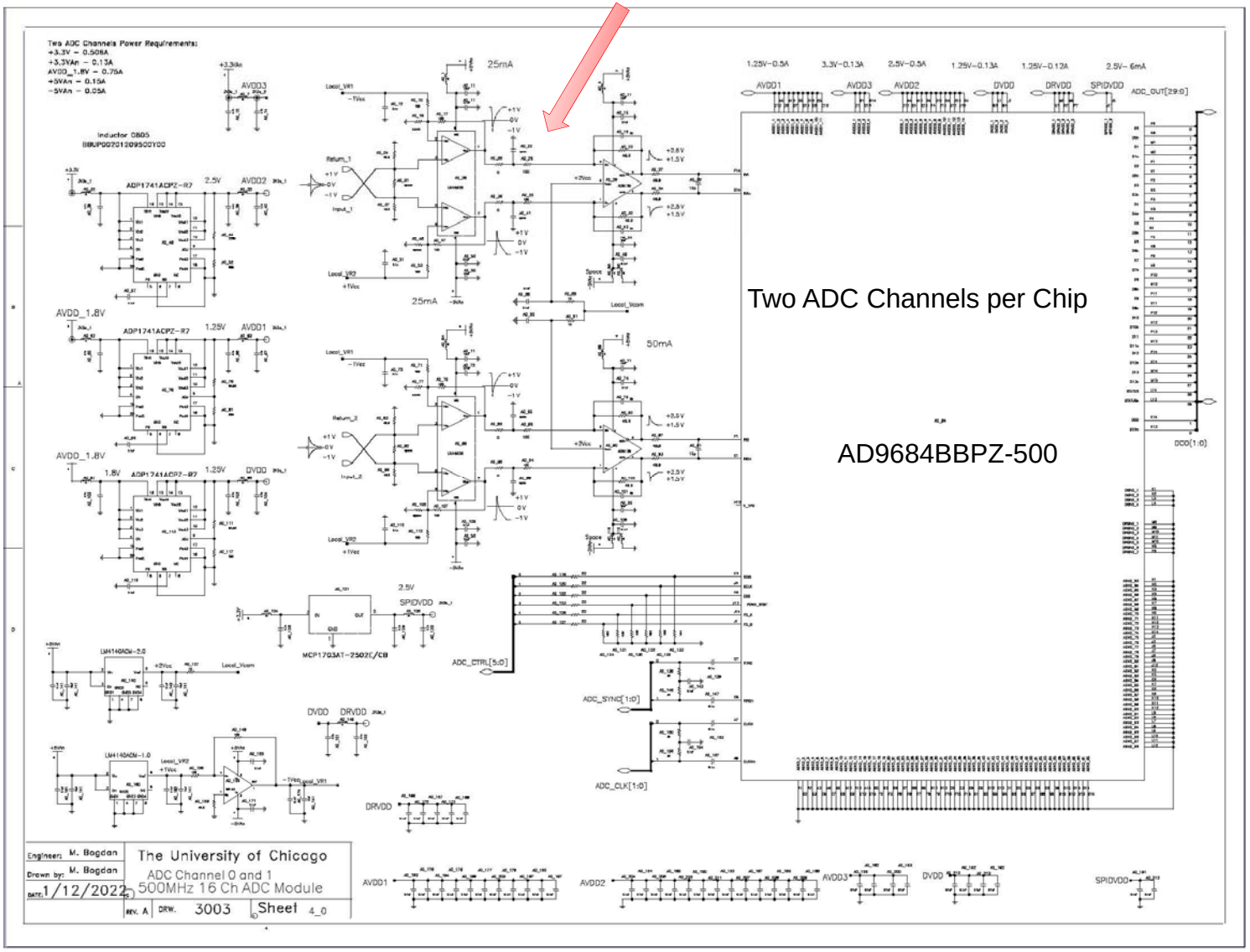
Same Front End Circuit as Old 500MHz ADC Module



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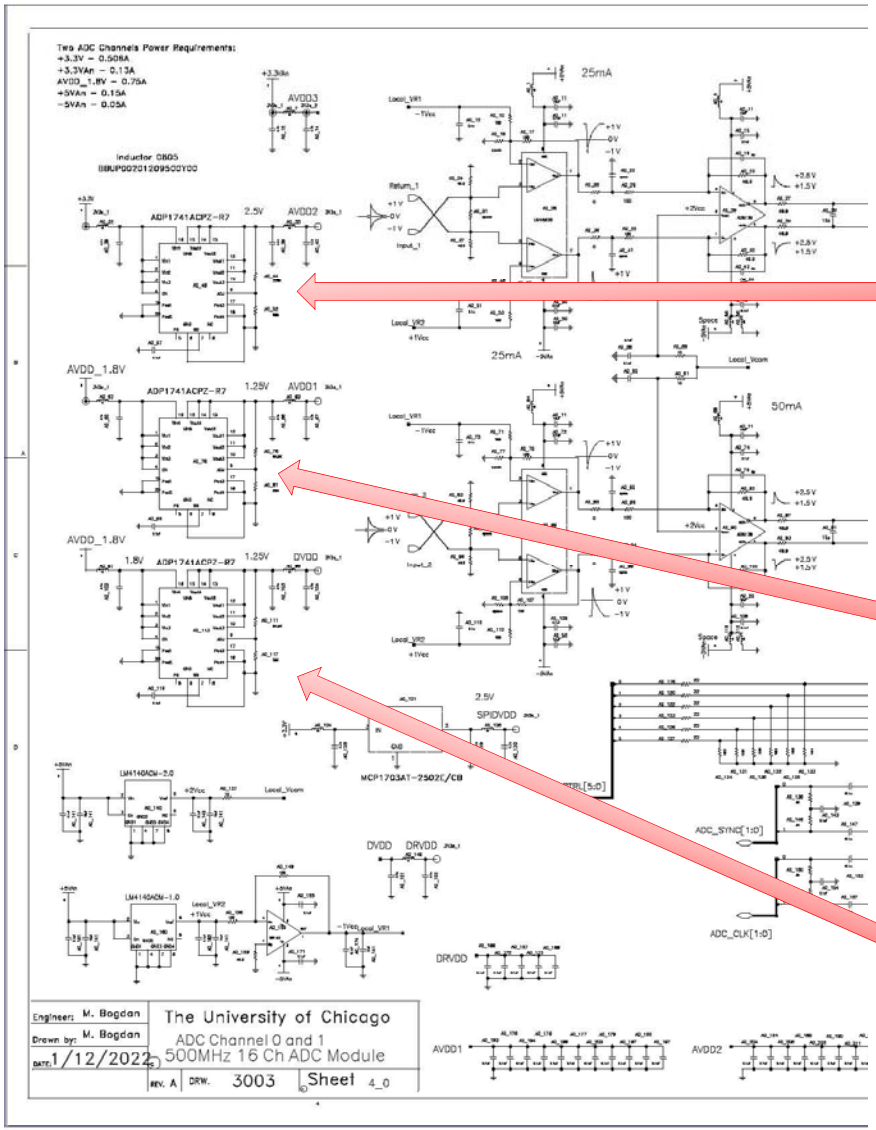
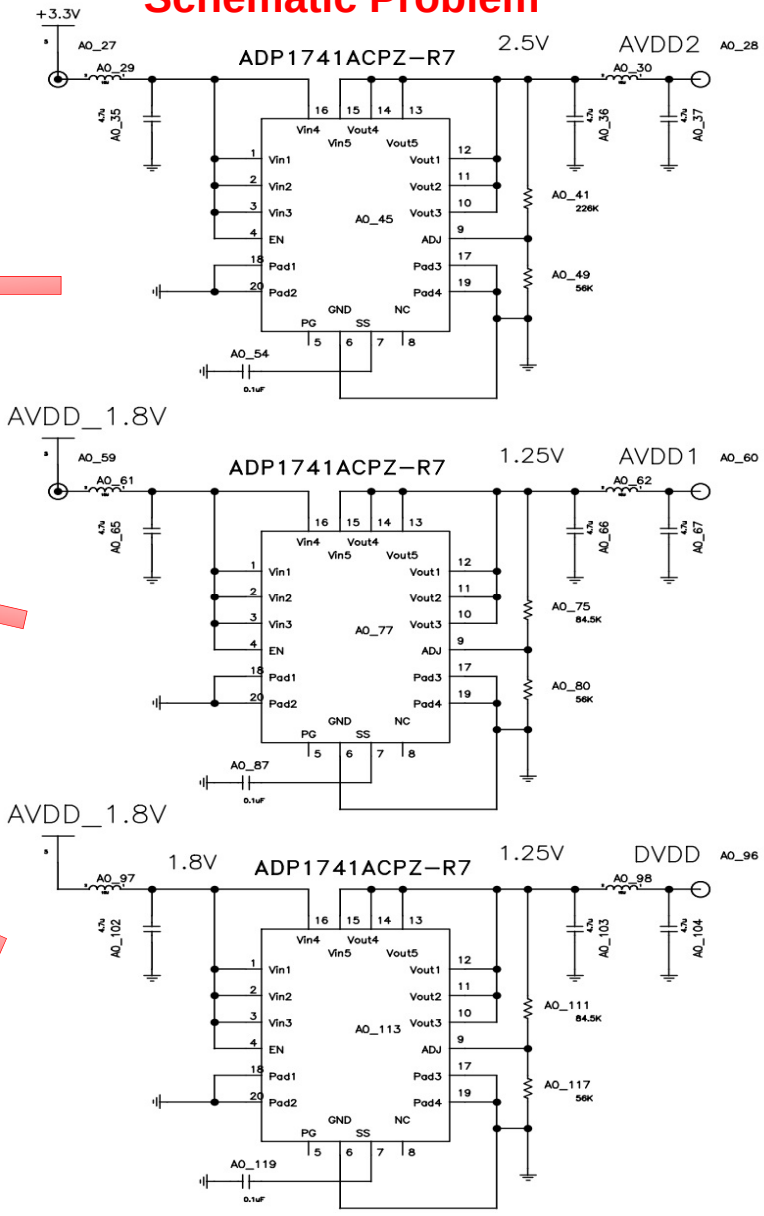


Schematic Problem



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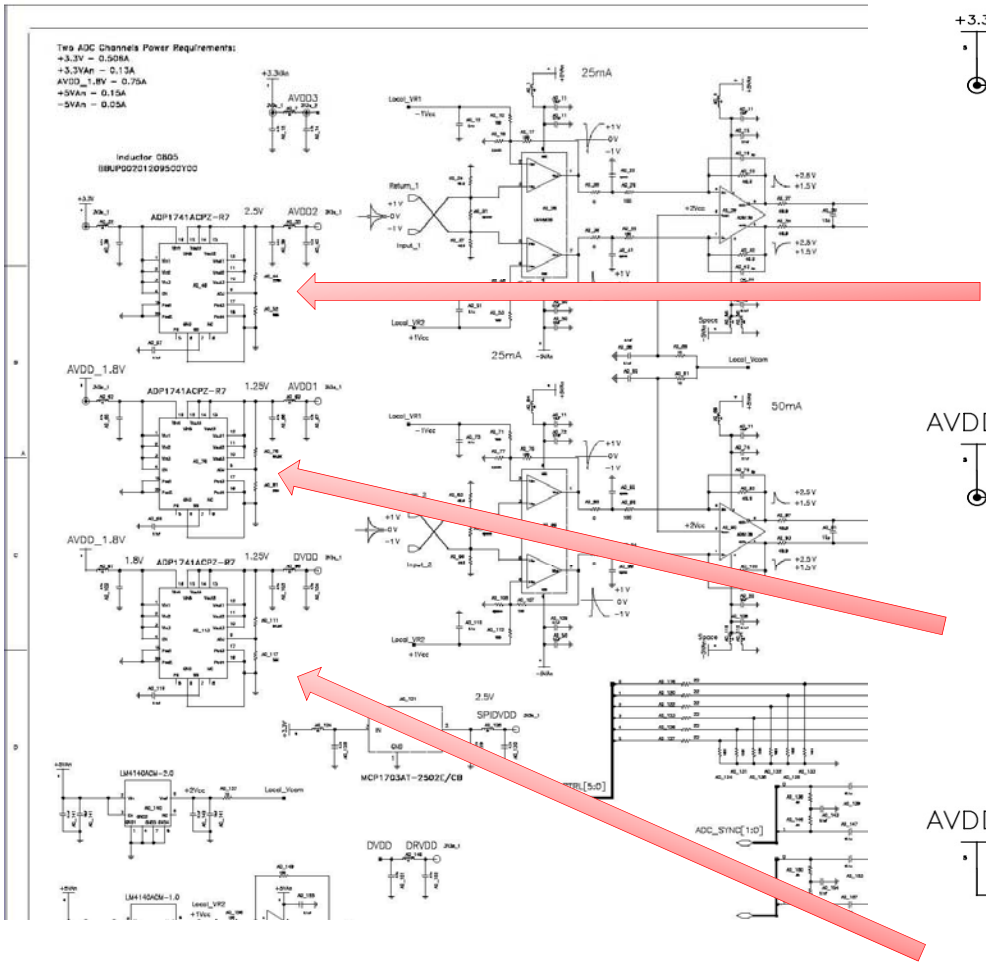

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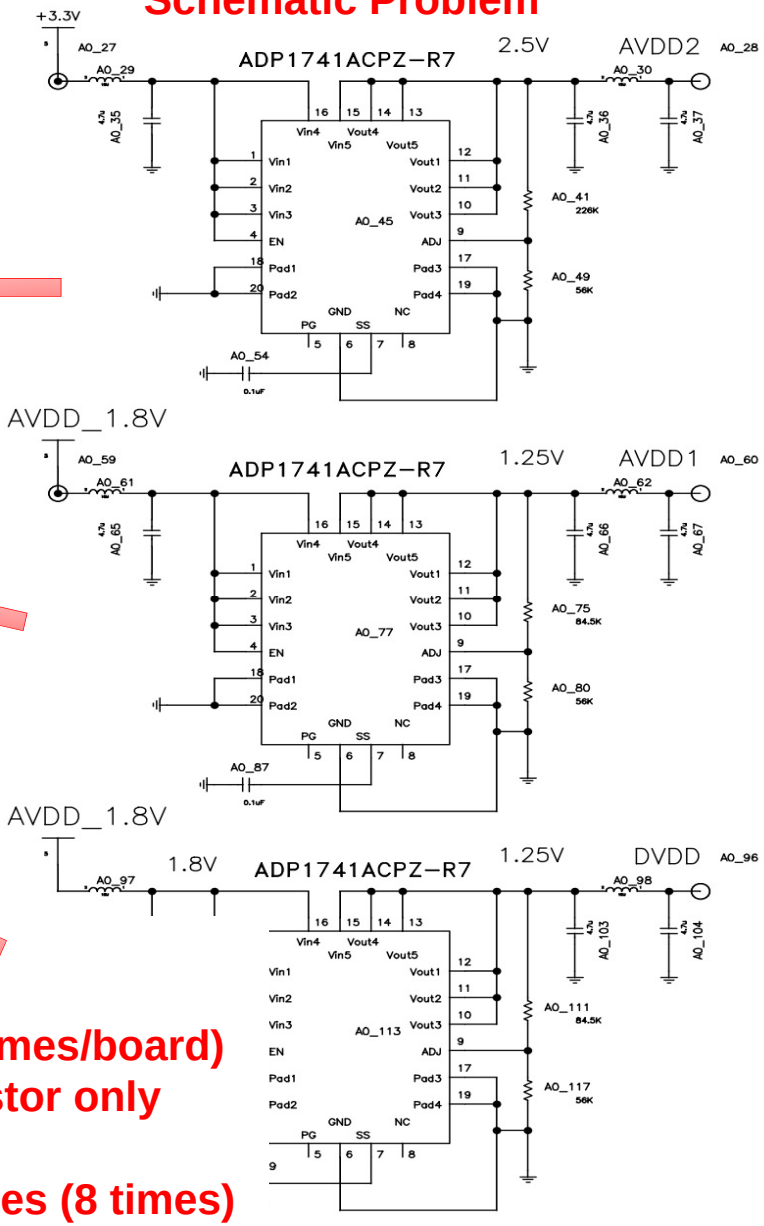

Connection Fix:

- **Remove output inductors for these 3 LDOs (8 times/board)**
- **Change AVDD_1.8V to 1.25V = change one resistor only**
- **Bypass 2 LDOs with wires (8 times)**
- **Bring 2.5V from other side of the board with wires (8 times)**

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ADC chip AD9684 - Data Sheet Problem 1:

Data Sheet: Chip starts in “one converter mode”, and internal register 0x568 needs to be changed from 0x00 to 0x01, to have two converters working.

Designed VME controlled SPI to change the ADC chip internal register.
Default value for internal register 0x568 is actually 0x01 and Data Sheets is Wrong!
ADC chips starts in two converter mode without register changes.
Data Sheet error was confirmed by AD technical support team.

AD9684 Data Sheet

Reg. Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x568	LVDS output mode	0	0	Frame clock mode (only used when in output data mode is in byte mode) 00 = frame clock always off 01 = frame clock always on 10 = reserved 11 = frame clock conditionally on based on PN23 sequence		0	Output data mode 000 = parallel mode (one converter) 001 = parallel interleaved mode (two converters) 010 = parallel channel multiplexed (even/odd) mode (one converter) 011 = parallel channel multiplexed (even/odd) mode (two converters) 100 = byte mode (one converter) 101 = byte mode (two converters) 110 = byte mode (four converters) Others = reserved			0x00	
0x569	Digital clock output adjust	0	0	0	0	0	0	DCO phase adjustment 0x0: 0° 0x1: 90° 0x2: 180° 0x3: 270°		0x01	

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ADC chip AD9684 - Data Sheet Problem 2:

Data Sheet: Chip sends a “Ramp output” when configured in test mode “1111”

Used VME controlled SPI to set the ADC chip in corresponding test mode.

Data Sheets is Wrong!
In that test mode, ADC chip sends out a counter, but every word is repeated 4 times!
This suggests a logic or a timing error in the FPGA design.
-> Time spent chasing inexistent hardware issue…

Data Sheet error was confirmed by AD technical support team.

Table 26. ADC Test Modes

Output Test Mode Bit Sequence	Pattern Name	Expression	Default/Seed Value	Sample (N, N + 1, N + 2, ...)
0000	Off (default)	Not applicable	Not applicable	Not applicable
0001	Midscale short	00 0000 0000 0000	Not applicable	Not applicable
0010	+Full-scale short	01 1111 1111 1111	Not applicable	Not applicable
0011	−Full-scale short	10 0000 0000 0000	Not applicable	Not applicable
0100	Checkerboard	10 1010 1010 1010	Not applicable	0x1555, 0x2AAA, 0x1555, 0x2AAA, 0x1555
0101	PN sequence long	$x^{23} + x^{18} + 1$	0x3AFF	0x3FD7, 0x0002, 0x26E0, 0x0A3D, 0x1CA6
0110	PN sequence short	$x^9 + x^5 + 1$	0x0092	0x125B, 0x3C9A, 0x2660, 0x0c65, 0x0697
0111	One-/zero-word toggle	11 1111 1111 1111	Not applicable	0x0000, 0x3FFF, 0x0000, 0x3FFF, 0x0000
1000	User input	Register 0x551 to Register 0x558	Not applicable	For repeat mode: User Pattern 1[15:2], User Pattern 2[15:2], User Pattern 3[15:2], User Pattern 4[15:2], User Pattern 1[15:2]… For single mode: User Pattern 1[15:2], User Pattern 2[15:2], User Pattern 3[15:2], User Pattern 4[15:2], 0x0000…
1111	Ramp output	(x) % 2^{14}	Not applicable	(x) % 2^{14}, (x + 1) % 2^{14}, (x + 2) % 2^{14}, (x + 3) % 2^{14}

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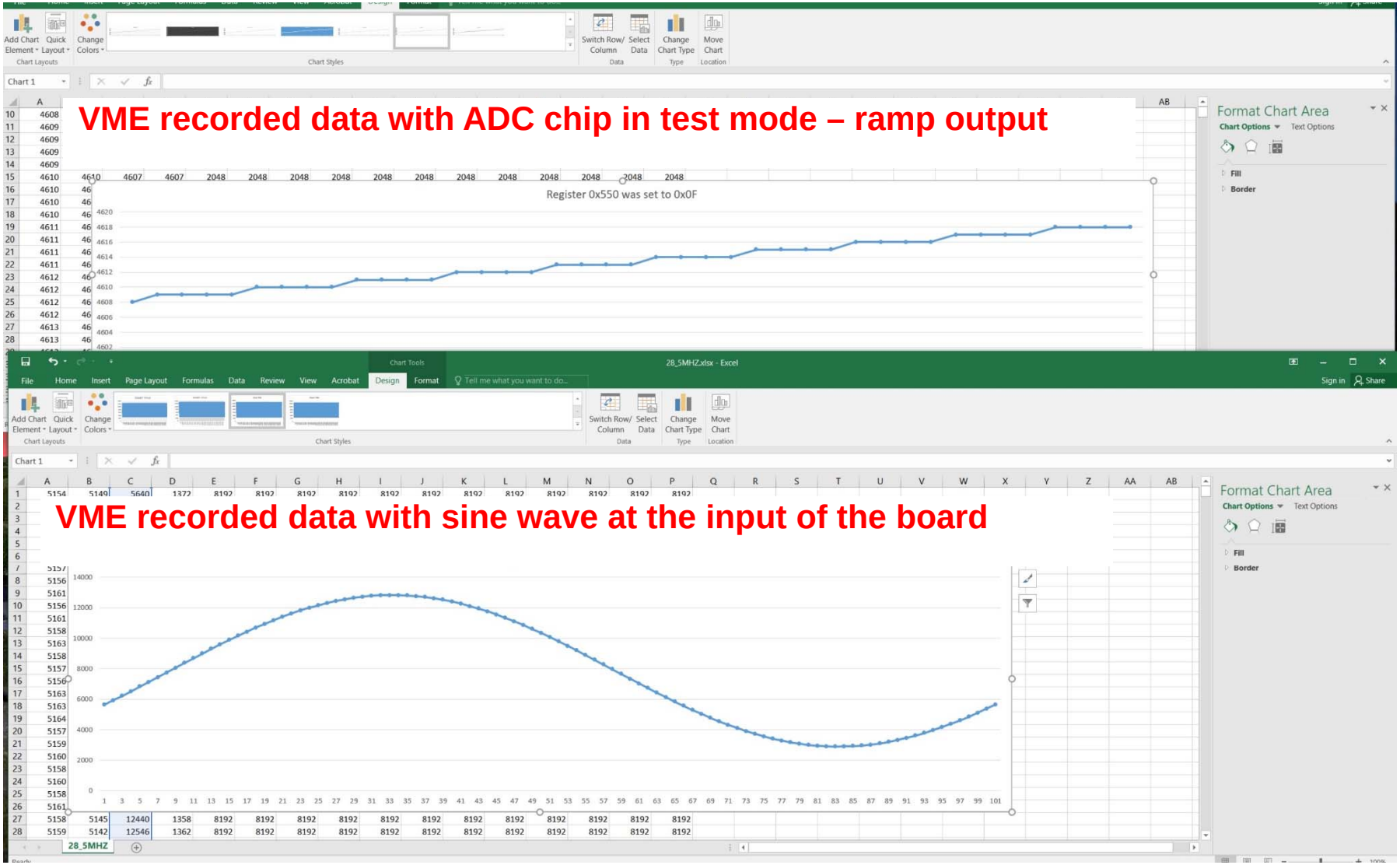
ADC chip AD9684 - Data Sheet Problem 2:



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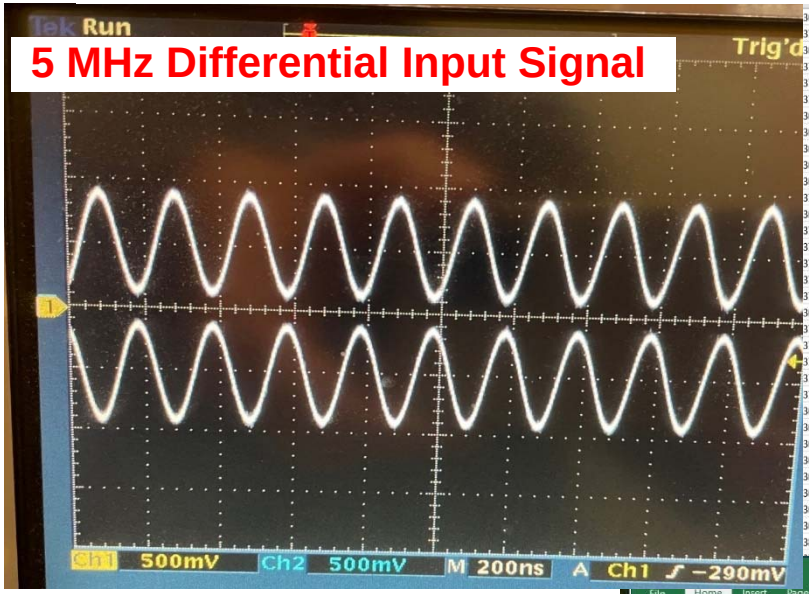
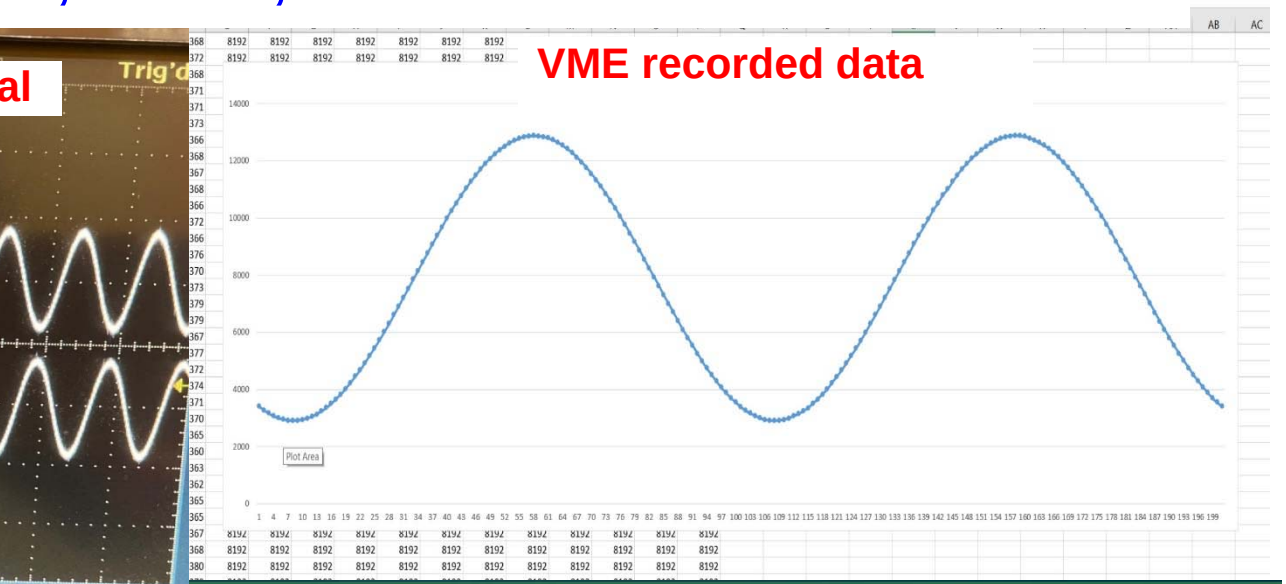
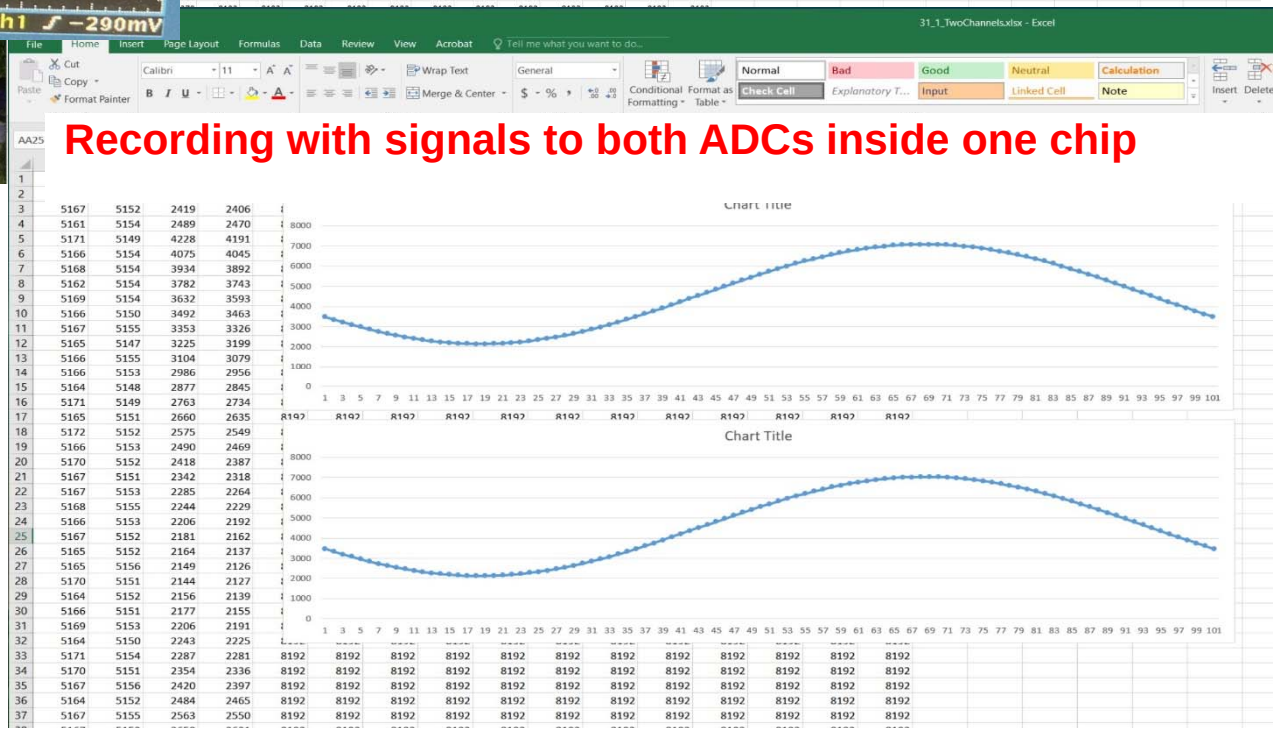


5 MHz Differential Input Signal

VME recorded data



Recording with signals to both ADCs inside one chip



Preliminary Tests:

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To do:

- **Install 8 ADC chips (16 channels) on the 2nd module**

- **Continue testing:**
  - **Total Power, Noise, X-talk etc.**