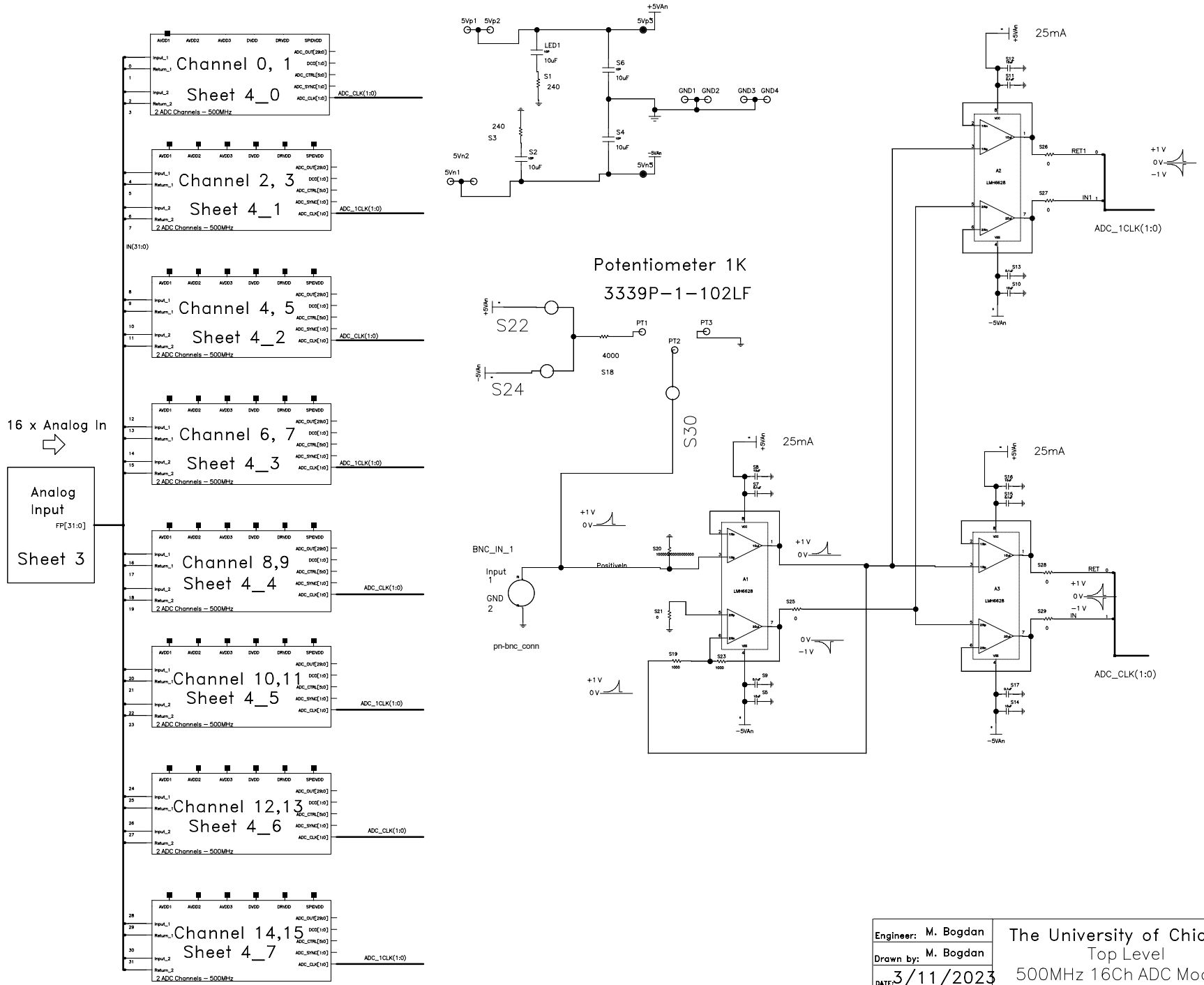
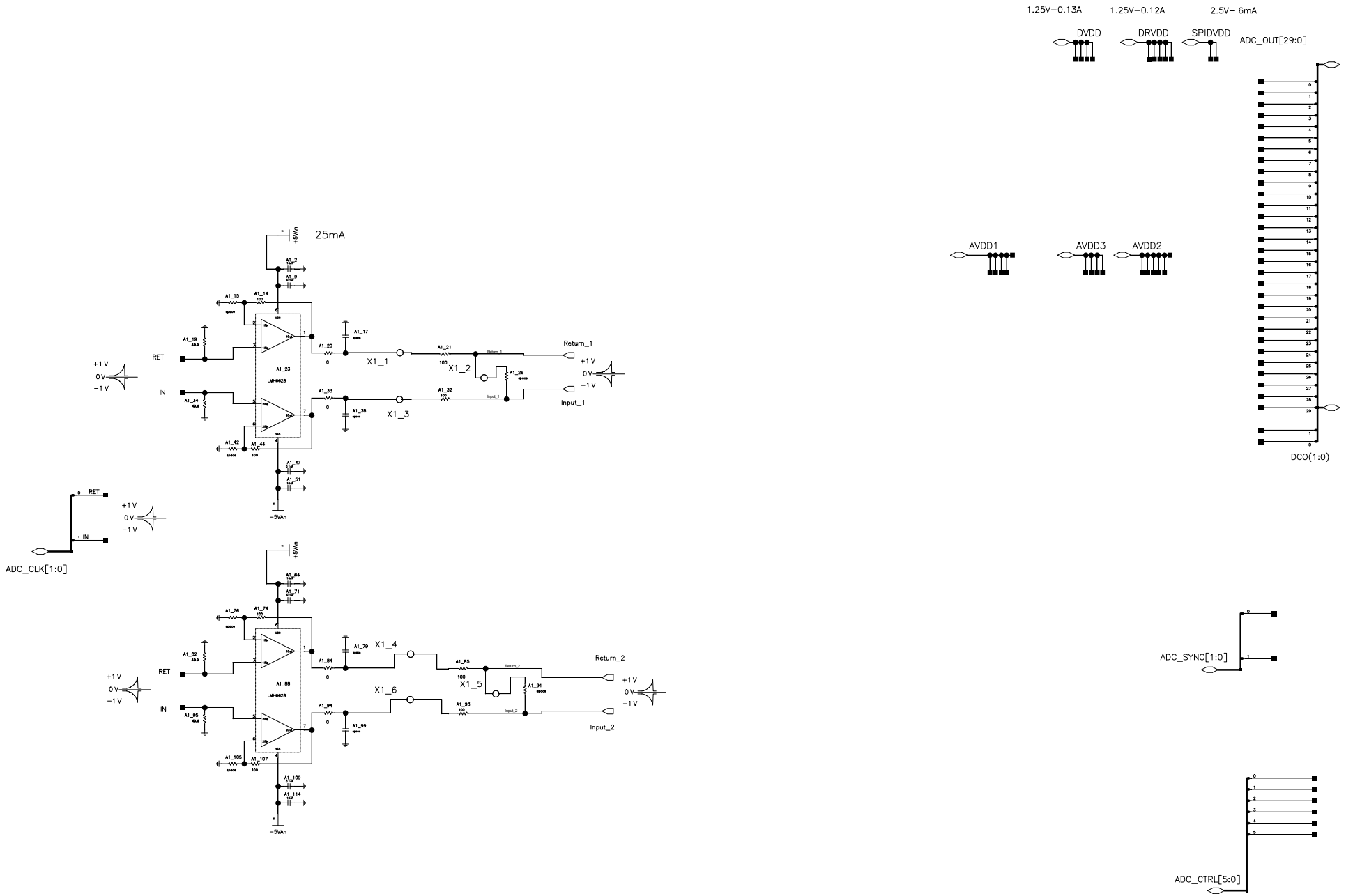
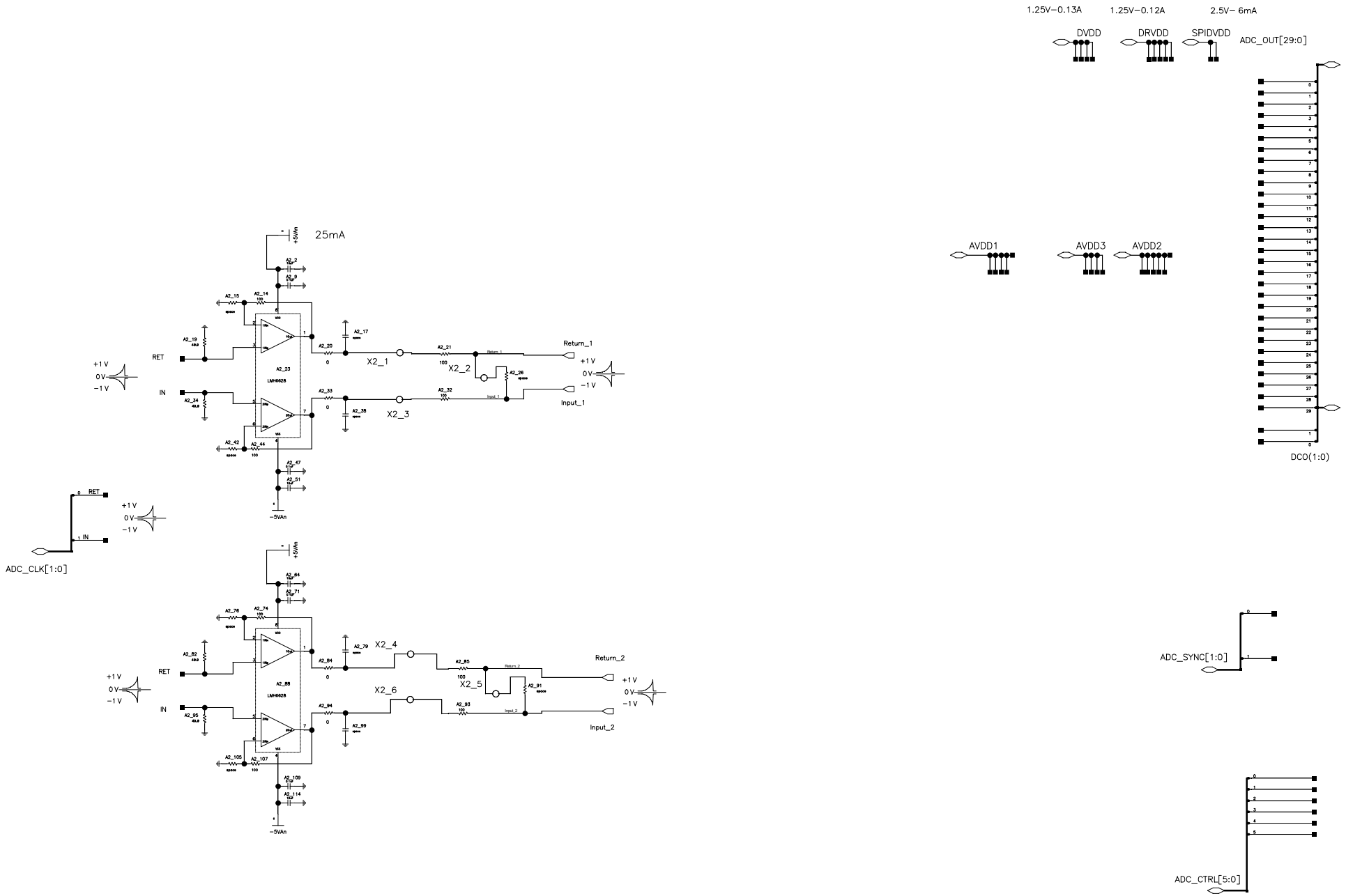


SCH# 3003
SPC# 3004
ASM# 3005

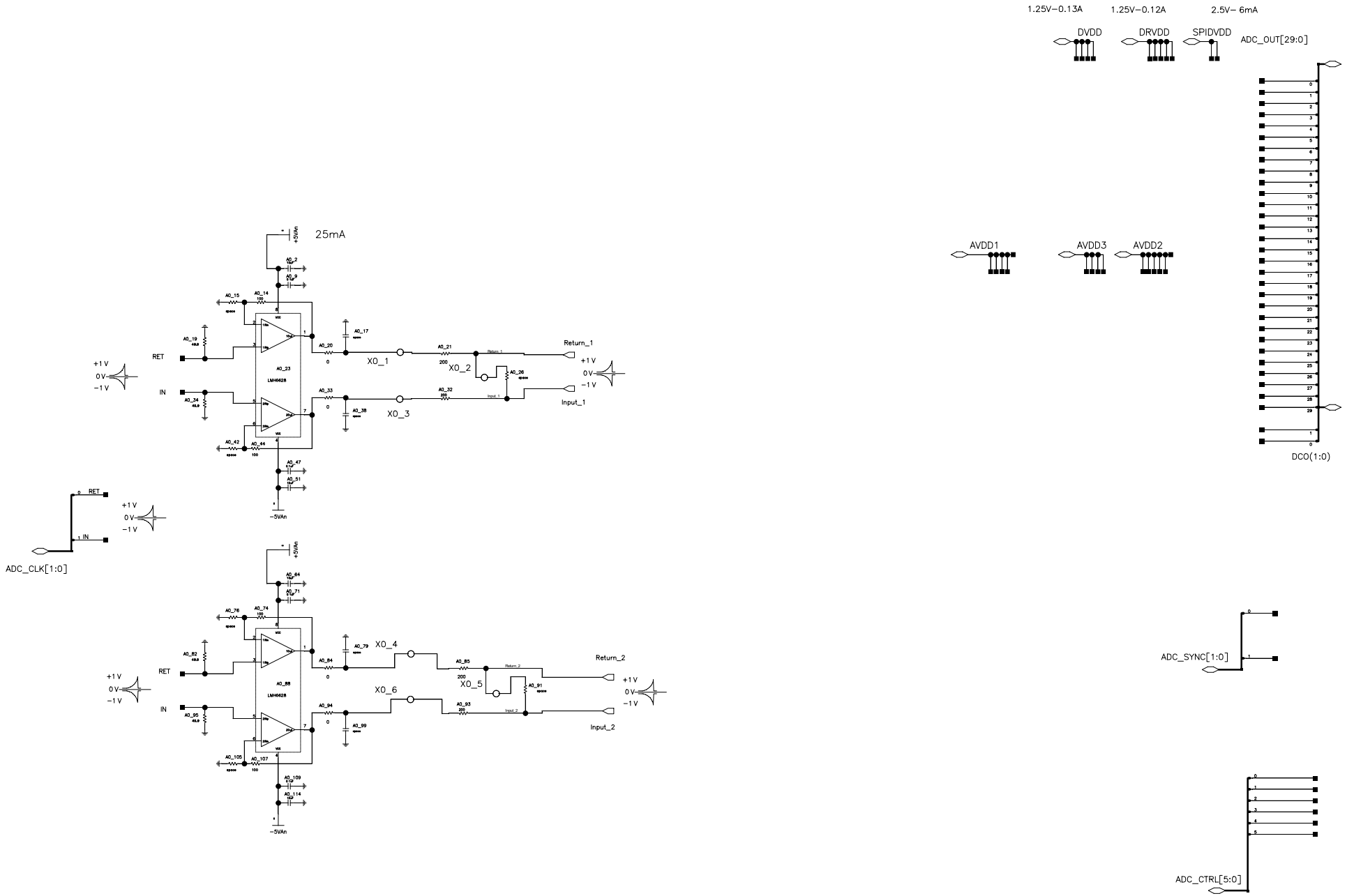
Engineer: M. Bogdan	The University of Chicago	
Drawn by: M. Bogdan	Top Level	
DATE: 3/11/2023	500MHz 16Ch ADC Module	
REV. A	DRW. 3003	Sheet 1



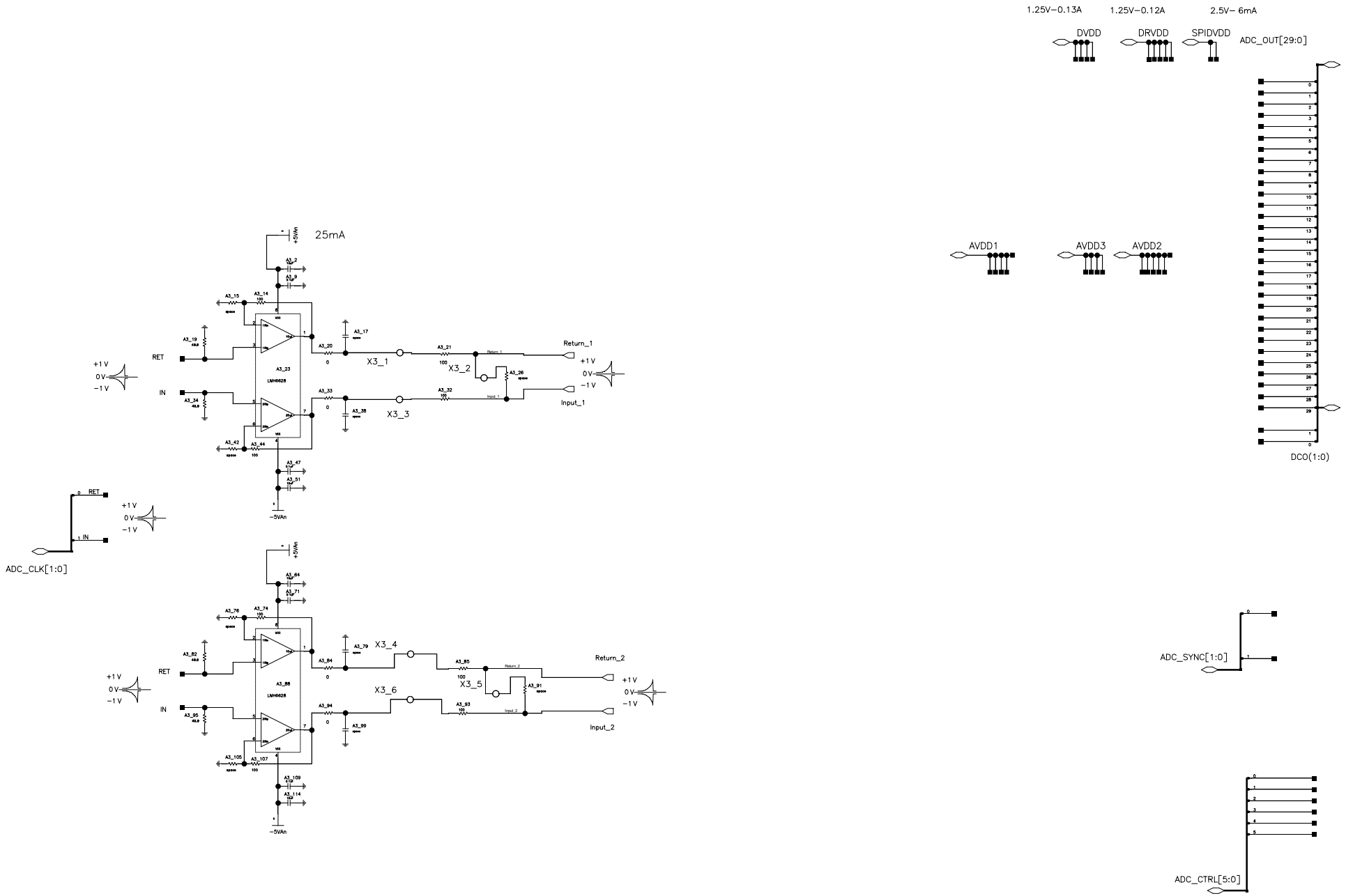
Engineer: M. Bogdan	The University of Chicago	
Drawn by: M. Bogdan	ADC Channel 0 and 1	
DATE: 3/11/2023	500MHz 16 Ch ADC Module	
REV. A	DRW. 3003	Sheet 4_0



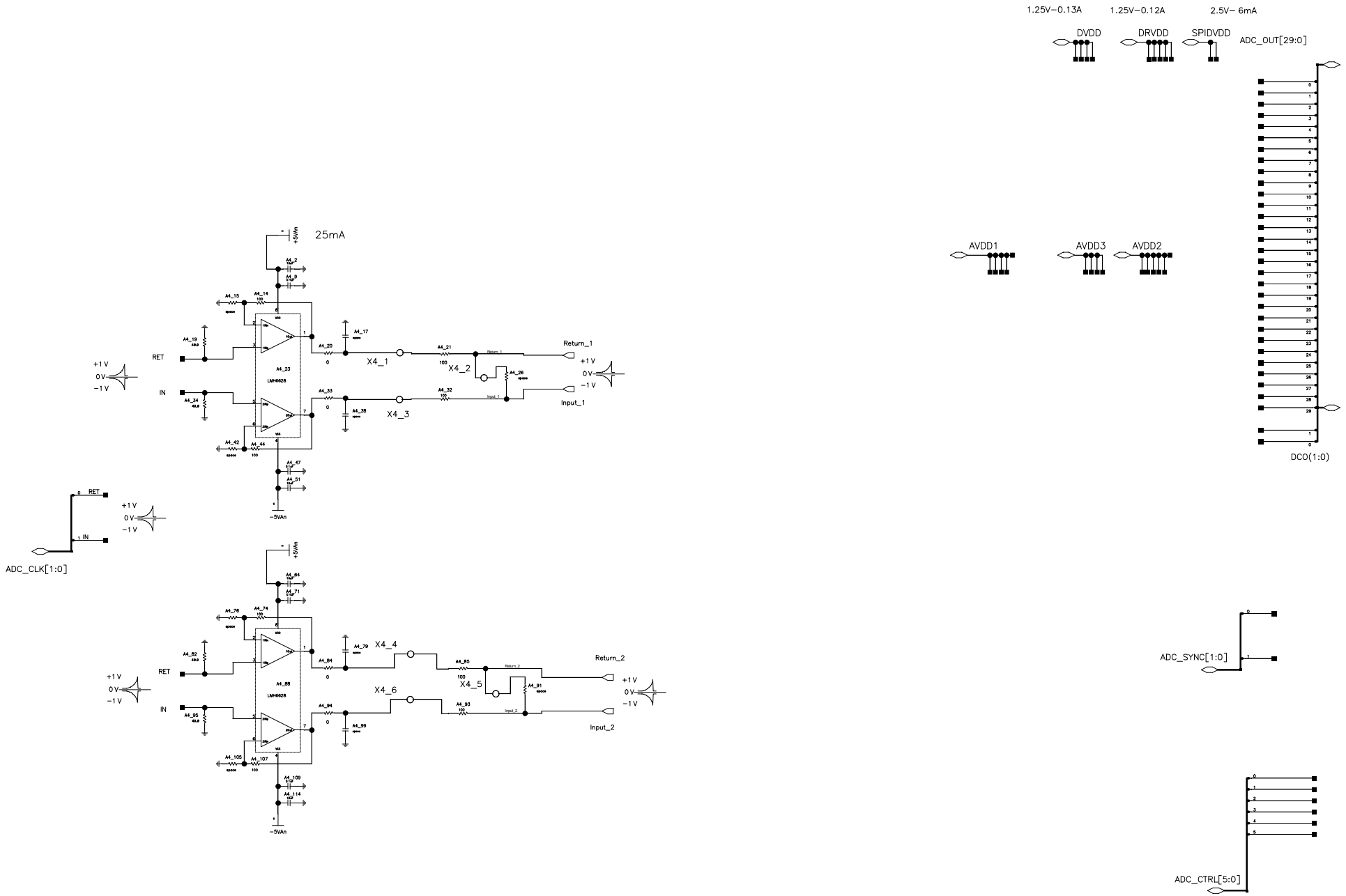
Engineer: M. Bogdan	The University of Chicago	
Drawn by: M. Bogdan	ADC Channel 0 and 1	
DATE: 3/11/2023	500MHz 16 Ch ADC Module	
REV. A	DRW. 3003	Sheet 4_0



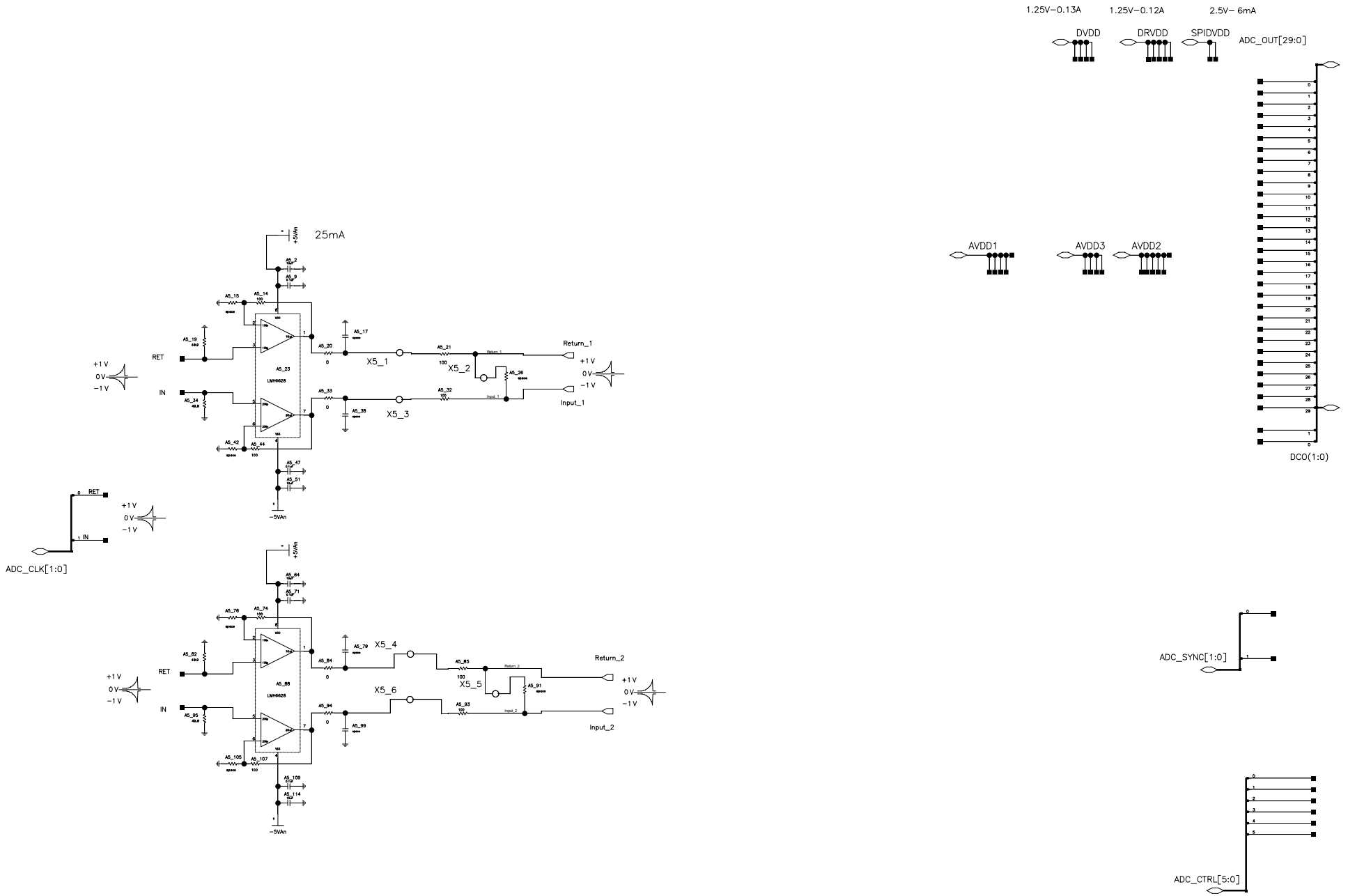
Engineer: M. Bogdan	The University of Chicago	
Drawn by: M. Bogdan	ADC Channel 0 and 1	
DATE: 3/11/2023	500MHz 16 Ch ADC Module	
REV. A	DRW. 3003	Sheet 4_0



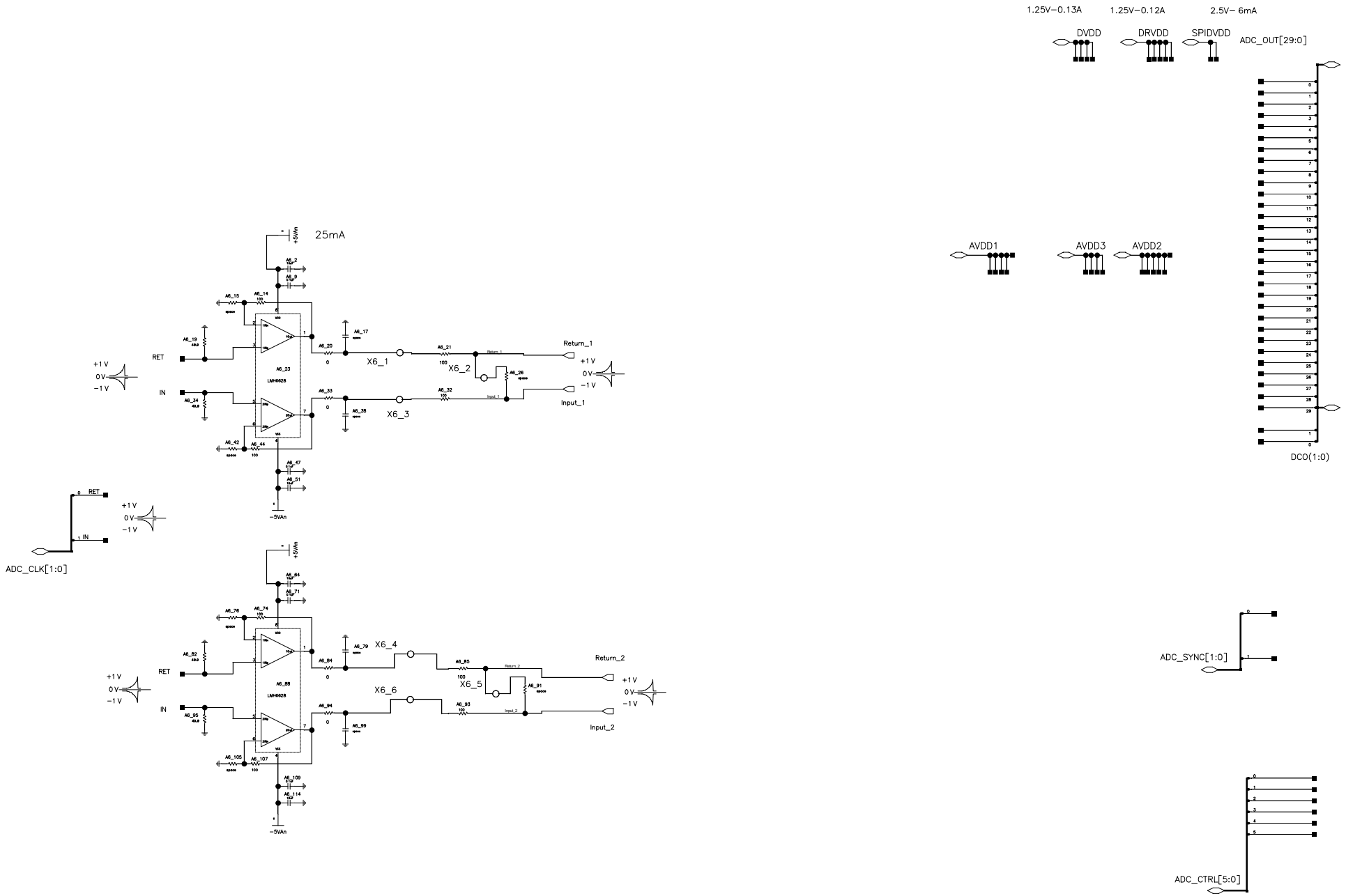
Engineer: M. Bogdan	The University of Chicago	
Drawn by: M. Bogdan	ADC Channel 0 and 1	
DATE: 3/11/2023	500MHz 16 Ch ADC Module	
REV. A	DRW. 3003	Sheet 4_0



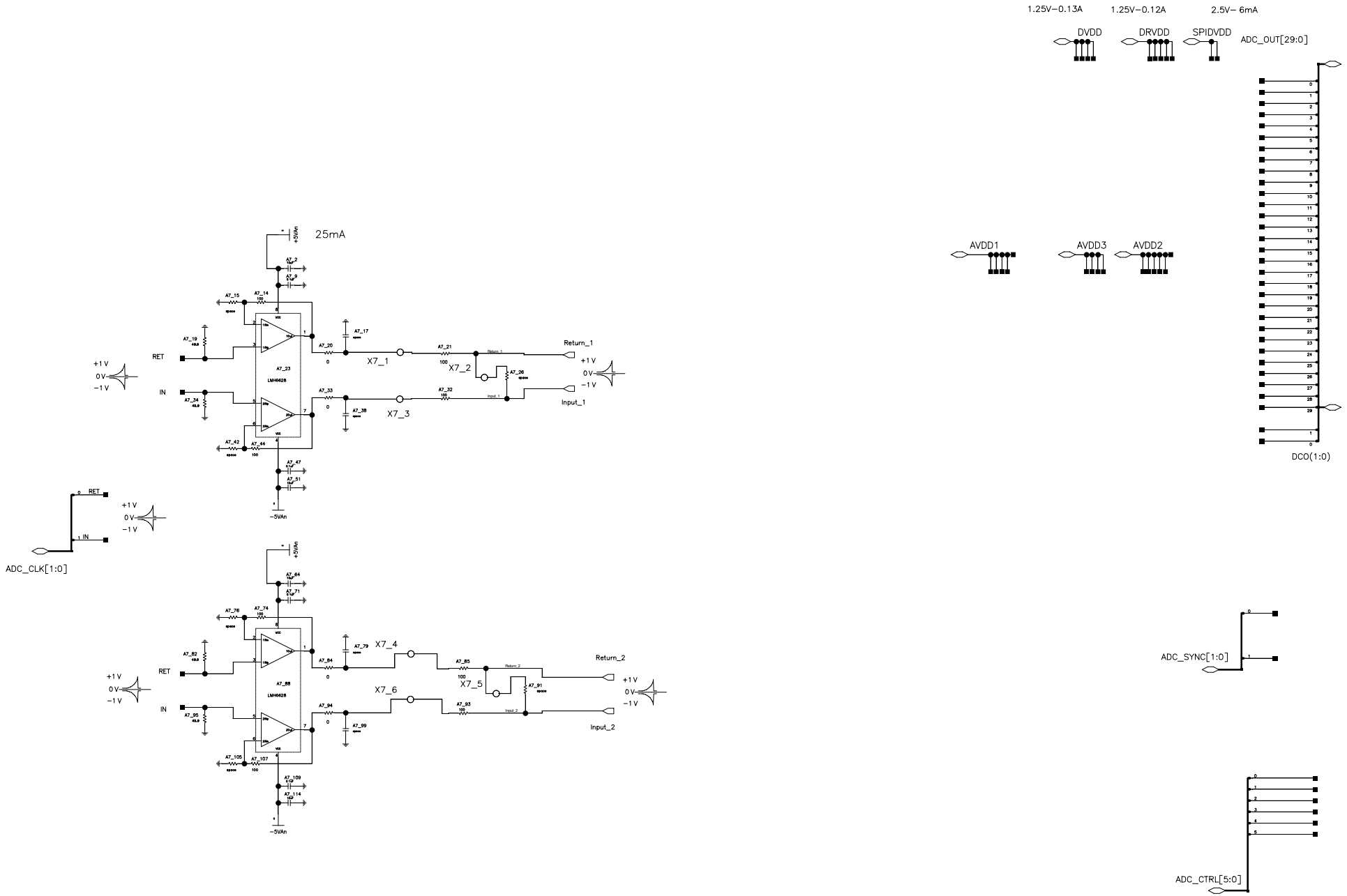
Engineer: M. Bogdan	The University of Chicago	
Drawn by: M. Bogdan	ADC Channel 0 and 1	
DATE: 3/11/2023	500MHz 16 Ch ADC Module	
REV. A	DRW. 3003	Sheet 4_0



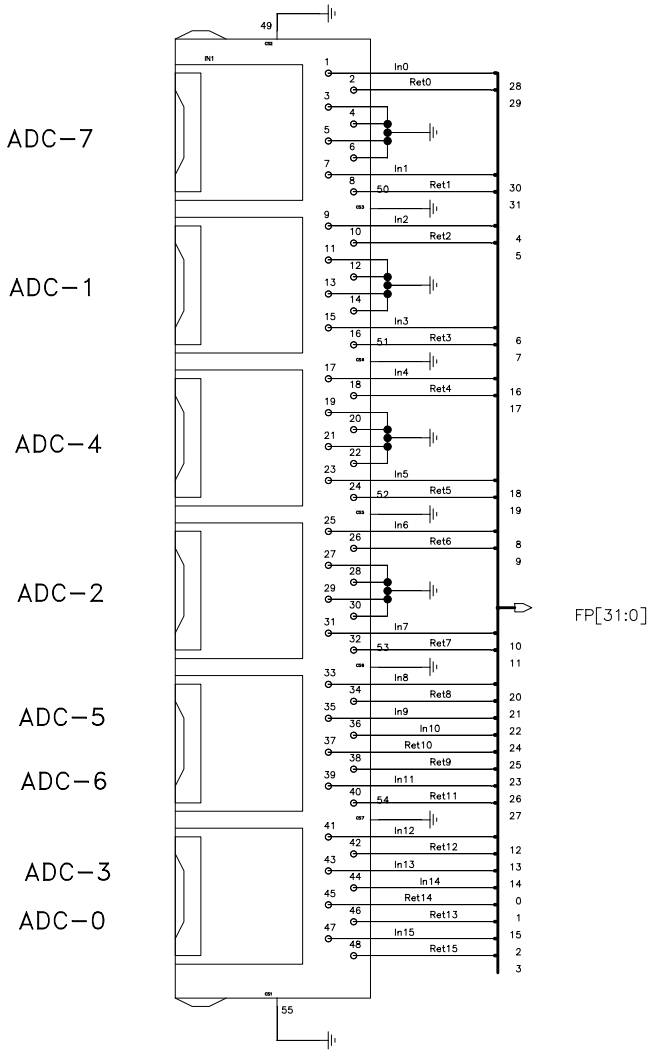
Engineer: M. Bogdan	The University of Chicago	
Drawn by: M. Bogdan	ADC Channel 0 and 1	
DATE: 3/11/2023	500MHz 16 Ch ADC Module	
REV. A	DRW. 3003	Sheet 4_0



Engineer: M. Bogdan	The University of Chicago	
Drawn by: M. Bogdan	ADC Channel 0 and 1	
DATE: 3/11/2023	500MHz 16 Ch ADC Module	
REV. A	DRW. 3003	Sheet 4_0



Engineer: M. Bogdan	The University of Chicago	
Drawn by: M. Bogdan	ADC Channel 0 and 1	
DATE: 3/11/2023	500MHz 16 Ch ADC Module	
REV. A	DRW. 3003	Sheet 4_0



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Engineer: M. Bogdan	The University of Chicago		
Drawn by: M. Bogdan	Analog Input Connector 1		
DATE: 2/6/2022	500MHz 16Ch ADC Module		
	REV. A	DRW. 3003	Sheet 3