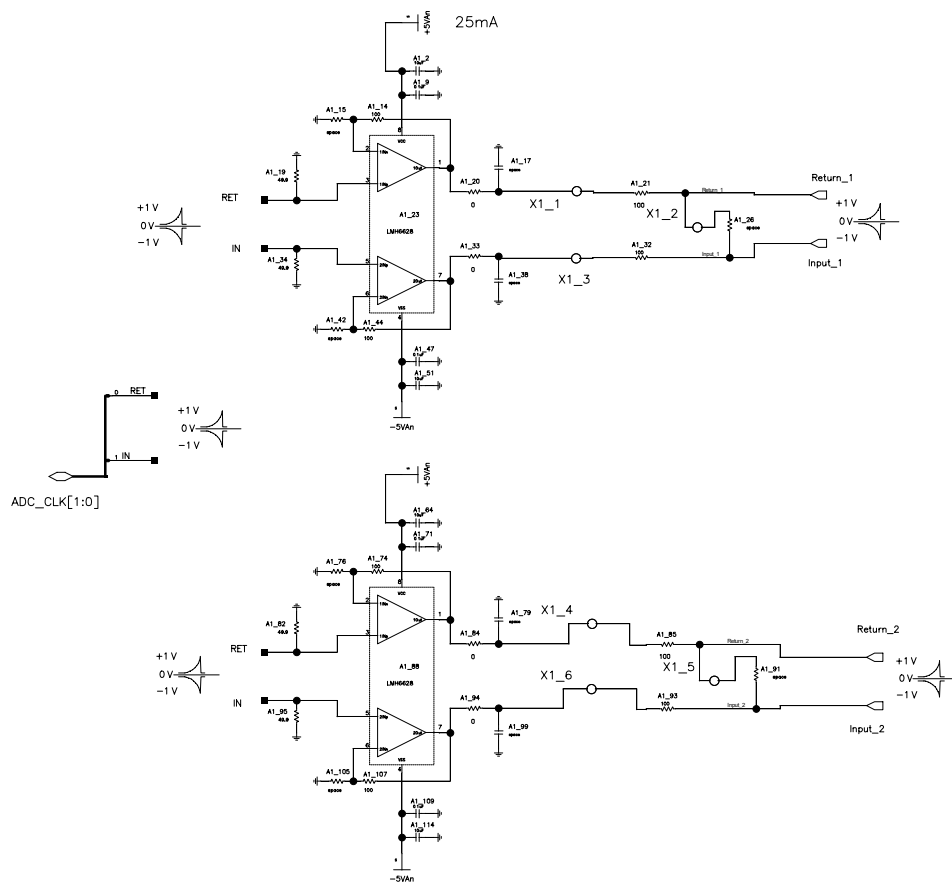
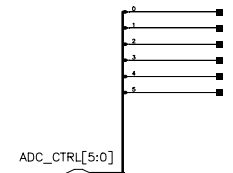
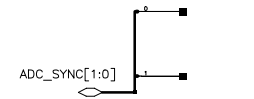
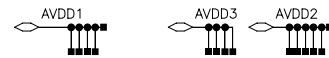
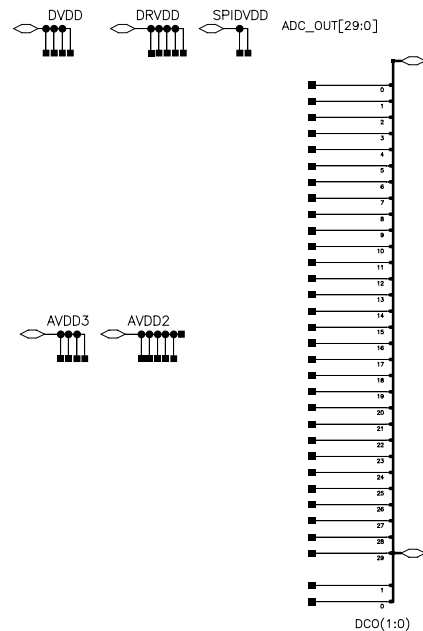


SCH# 3003
 SPC# 3004
 ASM# 3005

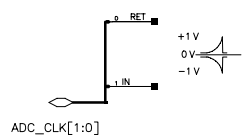
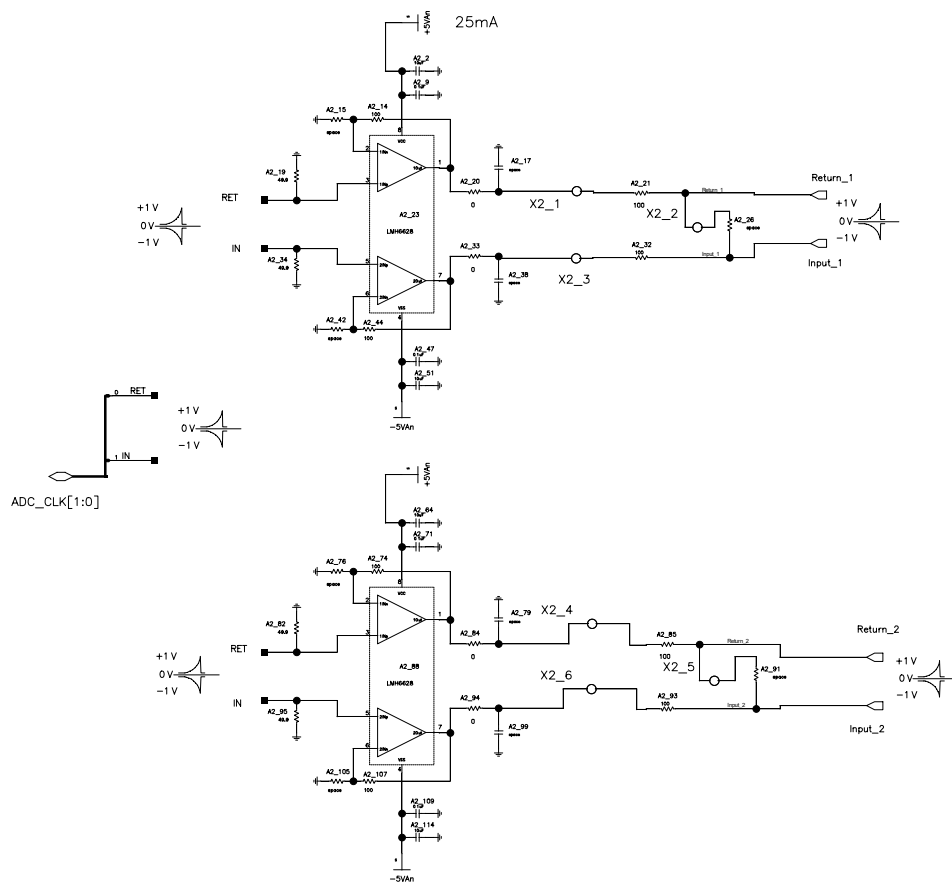
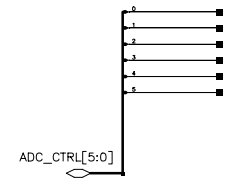
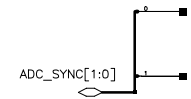
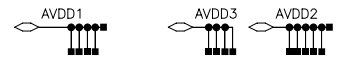
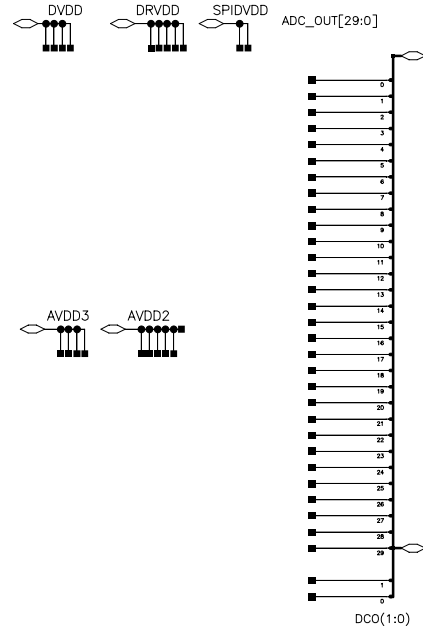
Engineer: M. Bogdan	The University of Chicago Top Level 500MHz 16Ch ADC Module
Drawn by: M. Bogdan	
DATE: 3/11/2023	
REV. A	DRW. 3003 Sheet 1

1.25V-0.13A 1.25V-0.12A 2.5V-6mA



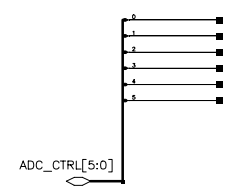
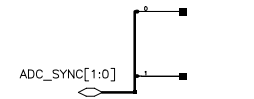
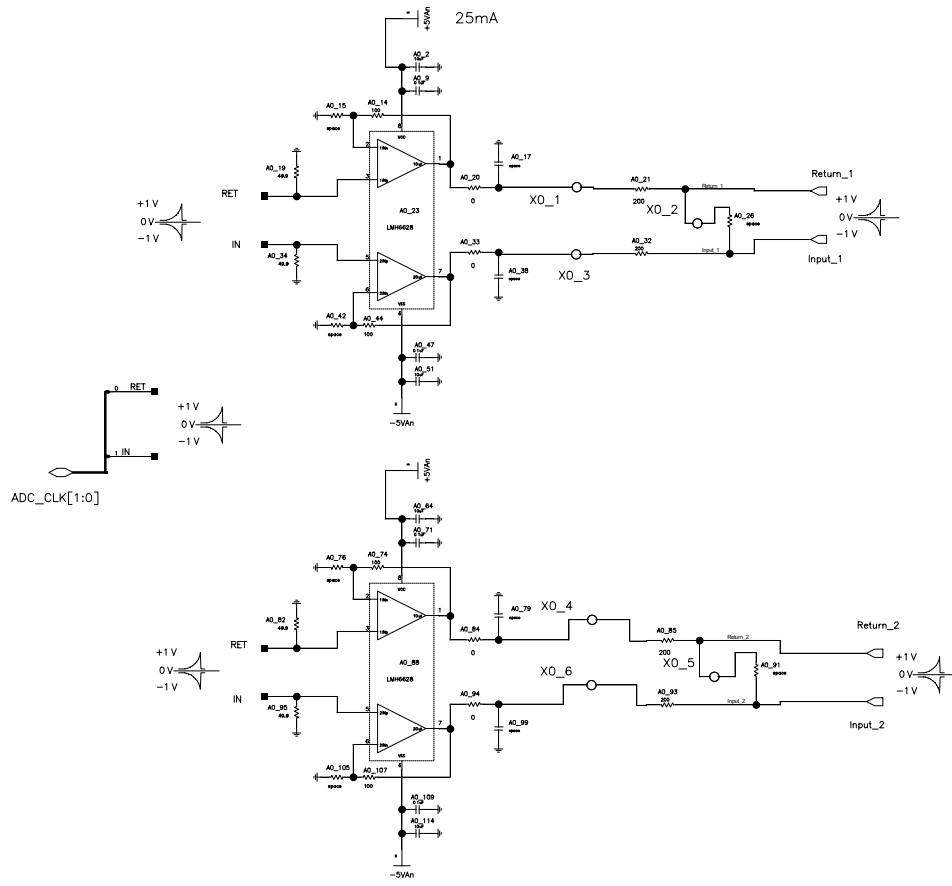
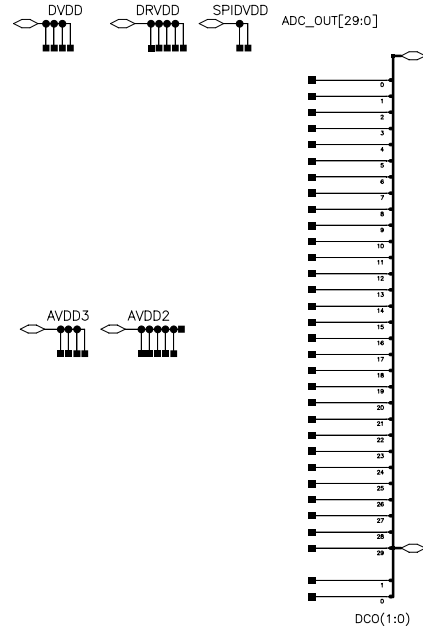
Engineer: M. Bogdan	The University of Chicago
Drawn by: M. Bogdan	ADC Channel 0 and 1
DATE: 3/11/2023	500MHz 16 Ch ADC Module
REV. A	DRW. 3003 Sheet 4_0

1.25V-0.13A 1.25V-0.12A 2.5V-6mA



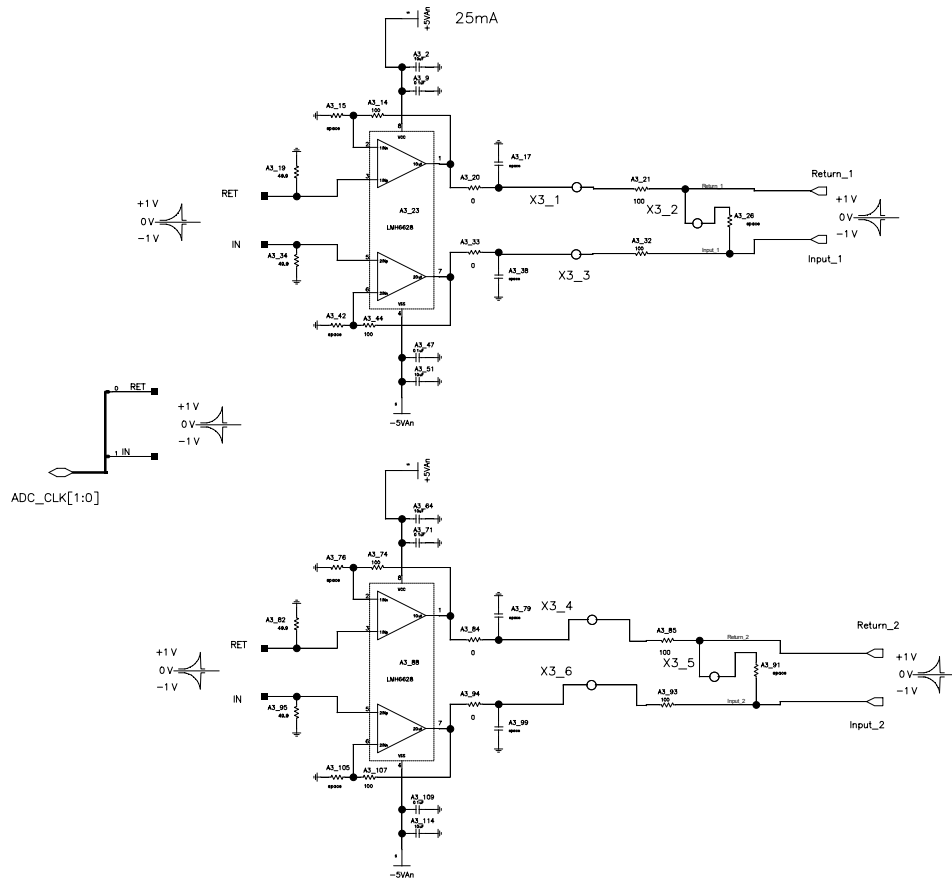
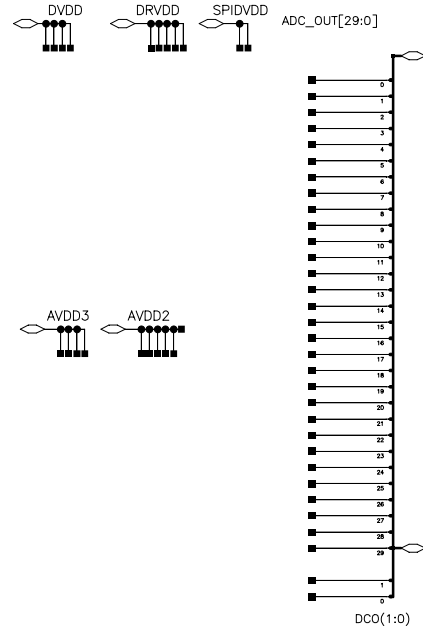
Engineer: M. Bogdan	The University of Chicago
Drawn by: M. Bogdan	ADC Channel 0 and 1
DATE: 3/11/2023	500MHz 16 Ch ADC Module
REV. A	DRW. 3003 Sheet 4_0

1.25V-0.13A 1.25V-0.12A 2.5V-6mA



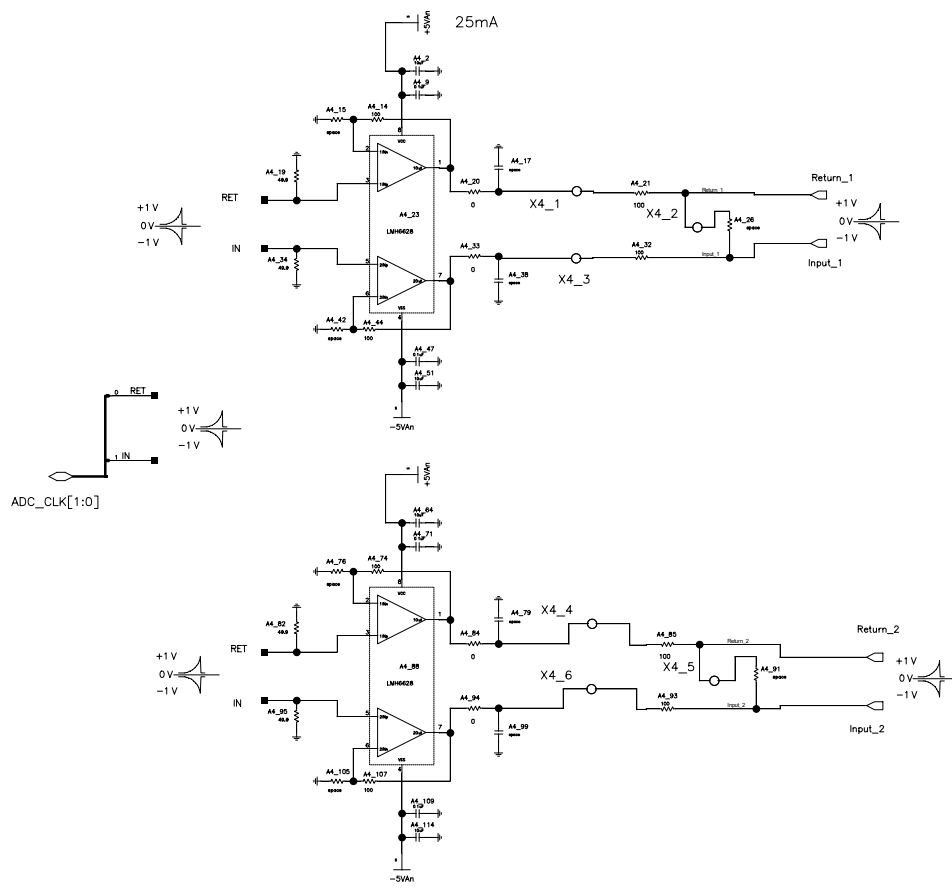
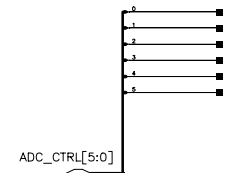
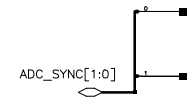
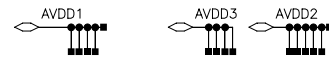
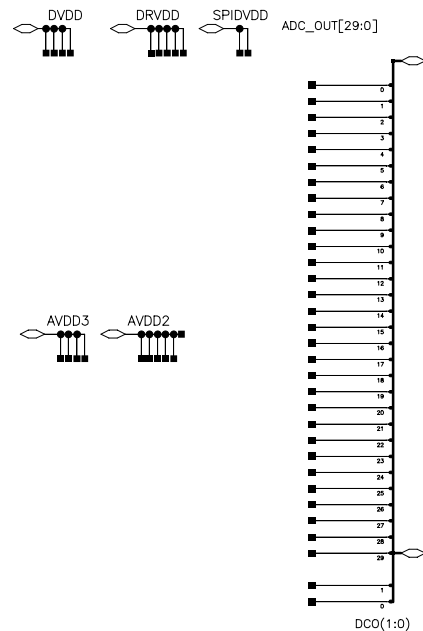
Engineer: M. Bogdan	The University of Chicago
Drawn by: M. Bogdan	ADC Channel 0 and 1
DATE: 3/11/2023	500MHz 16 Ch ADC Module
REV. A	DRW. 3003 Sheet 4_0

1.25V-0.13A 1.25V-0.12A 2.5V-6mA



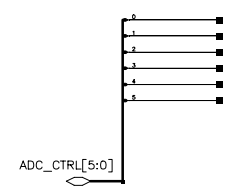
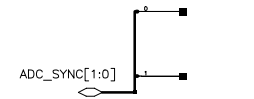
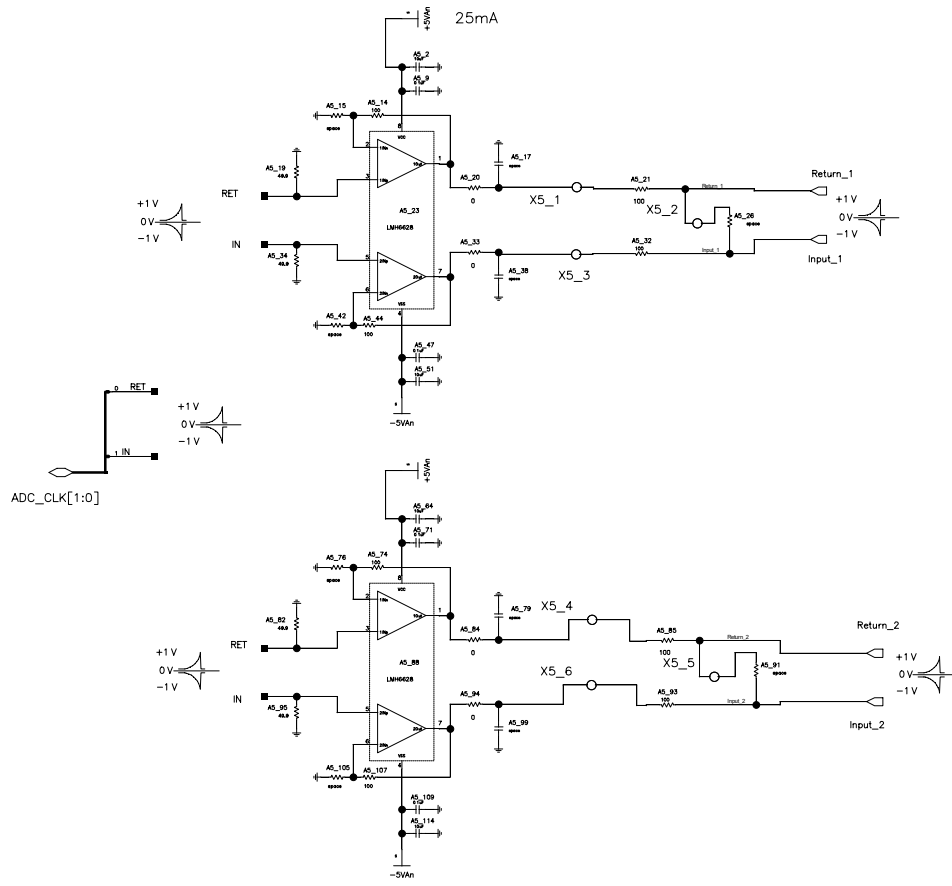
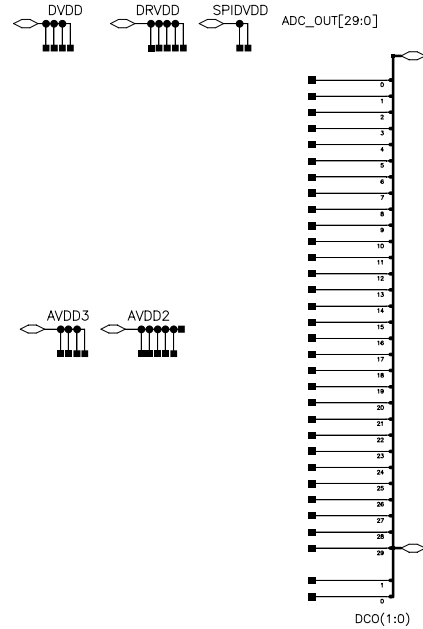
Engineer: M. Bogdan	The University of Chicago
Drawn by: M. Bogdan	ADC Channel 0 and 1
DATE: 3/11/2023	500MHz 16 Ch ADC Module
REV. A	DRW. 3003 Sheet 4_0

1.25V-0.13A 1.25V-0.12A 2.5V-6mA



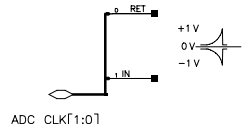
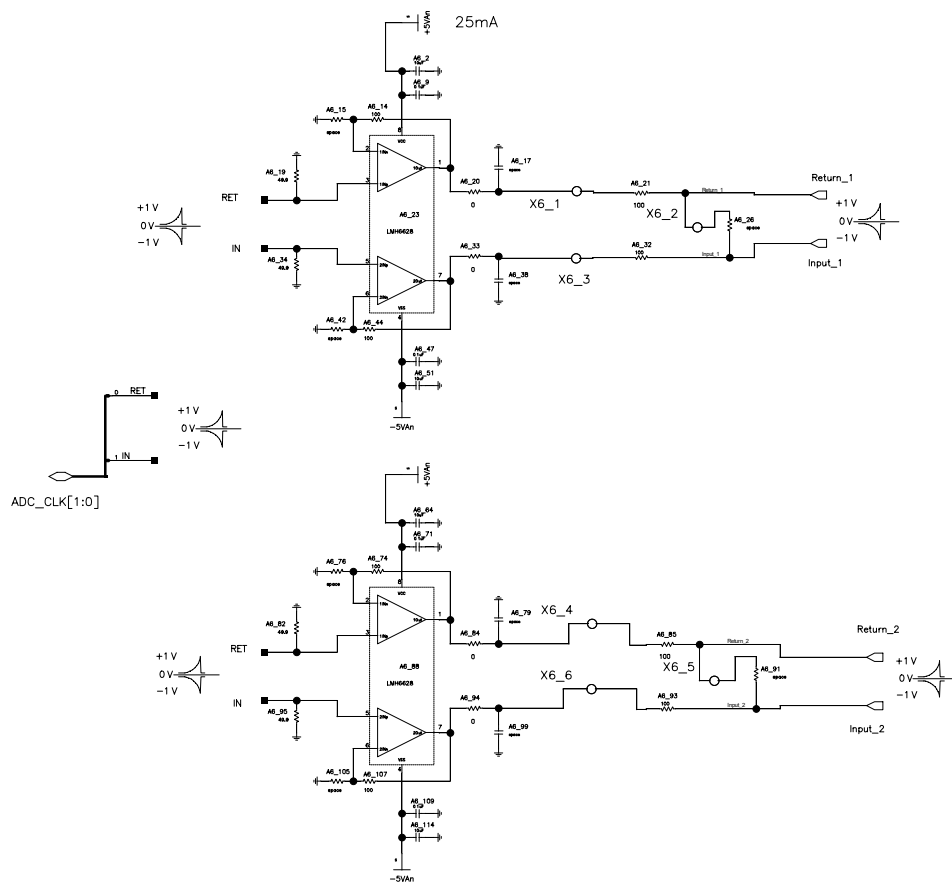
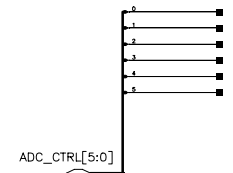
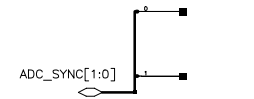
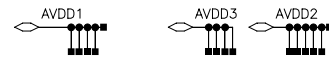
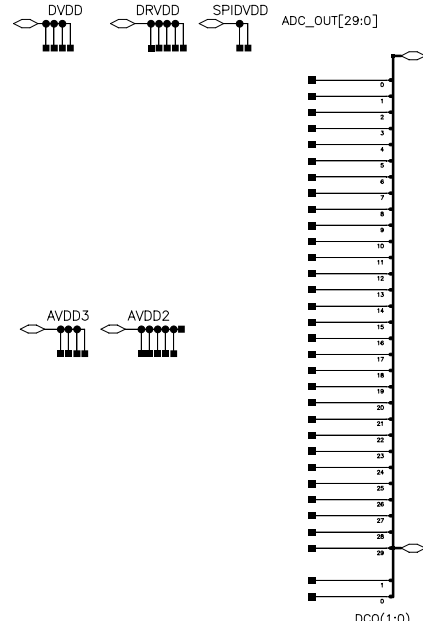
Engineer: M. Bogdan	The University of Chicago
Drawn by: M. Bogdan	ADC Channel 0 and 1
DATE: 3/11/2023	500MHz 16 Ch ADC Module
REV. A	DRW. 3003 Sheet 4_0

1.25V-0.13A 1.25V-0.12A 2.5V-6mA



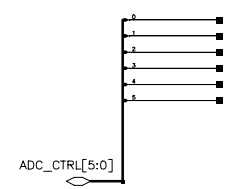
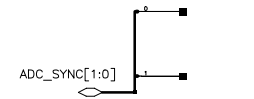
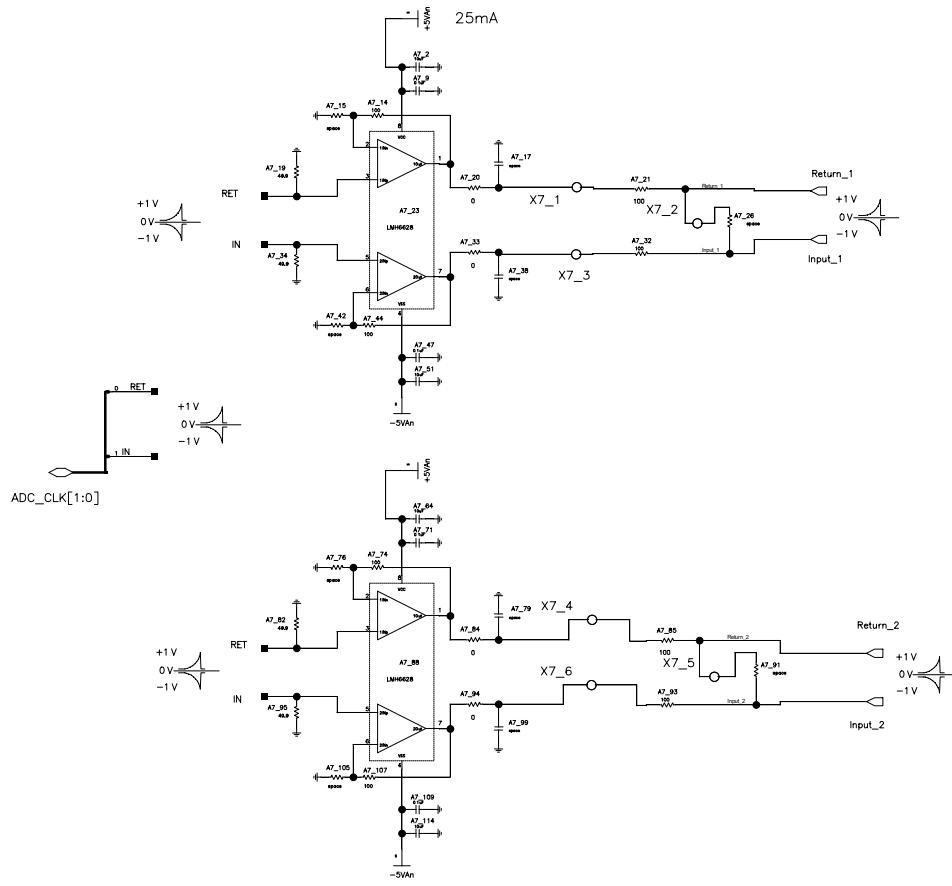
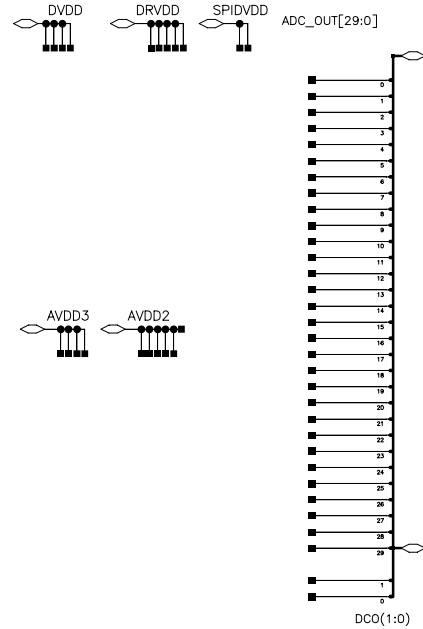
Engineer: M. Bogdan	The University of Chicago
Drawn by: M. Bogdan	ADC Channel 0 and 1
DATE: 3/11/2023	500MHz 16 Ch ADC Module
REV. A	DRW. 3003 Sheet 4_0

1.25V-0.13A 1.25V-0.12A 2.5V-6mA



Engineer: M. Bogdan	The University of Chicago
Drawn by: M. Bogdan	ADC Channel 0 and 1
DATE: 3/11/2023	500MHz 16 Ch ADC Module
REV. A	DRW. 3003 Sheet 4_0

1.25V-0.13A 1.25V-0.12A 2.5V-6mA



Engineer: M. Bogdan	The University of Chicago
Drawn by: M. Bogdan	ADC Channel 0 and 1
DATE: 3/11/2023	500MHz 16 Ch ADC Module
REV. A	DRW. 3003 Sheet 4_0

ADC-7

ADC-1

ADC-4

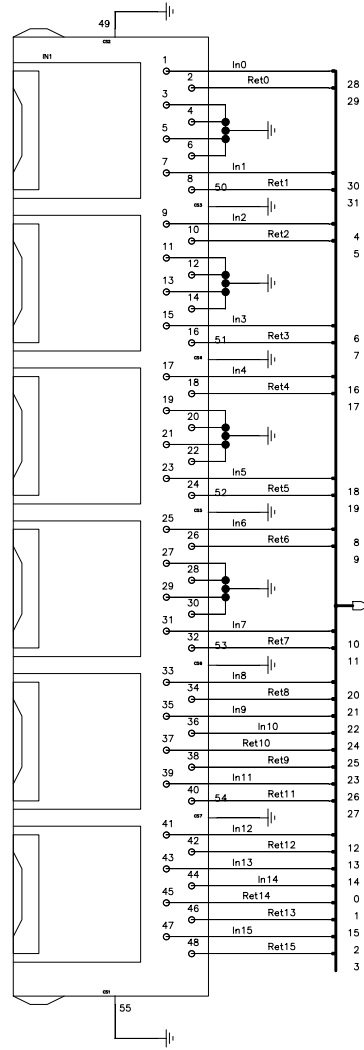
ADC-2

ADC-5

ADC-6

ADC-3

ADC-0



FP[31:0]

43223-8158

Engineer: M. Bogdan	The University of Chicago
Drawn by: M. Bogdan	Analog Input Connector 1
DATE: 2/6/2022	500MHz 16Ch ADC Module
REV. A	DRW. 3003 Sheet 3