

Data Acquisition System for a K_L Experiment at J-Parc

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Abstract

We present the proposed Data Acquisition (DAQ) system for KOTO, a $K_L \rightarrow \pi^0 \nu \nu$ experiment at J-Parc, Japan. It comprises two distinctive blocks: a 14(12)-bit, 125 (500) MHz ADC module for reading the approximately 4000 front-end channels; and a digital Trigger module able to provide a detector-wise synchronous energy sum. A Master Clock and Trigger Supervisor Module, with fans out of control signals to the whole system, completes the DAQ Architecture. The front-end readout board amplifies analog pulses from 16 photomultipliers and passes them through a 10-pole shaper before digitization. Data are then processed locally with field programmable gate arrays (FPGAs) to determine real-time energy values for the system Trigger Supervisor. The ADC module is provided with a pipeline, up to 4 μ s long, which stores the acquisitions, awaiting the system trigger pulse. After a trigger, data are packed and buffered on on-board memories for readout via the VME32/64 backplane. The full design and preliminary test results will be described.

I. SYSTEM ARCHITECTURE

We present the Data Acquisition (DAQ) System for the Step-1 phase of the KOTO experiment [1], a high energy physics kaon experiment at the Japan Particle Accelerator Research Complex (J-PARC). The goal of the experiment is to measure the rate of the rare decay $K_L \rightarrow \pi^0 \nu \nu$. This flavour changing neutral current decay is predicted by the Standard Model (SM) to happen only once every 3.3×10^{11} K_L decays. If not observed or observed at a rate very different from the SM predictions, it will shed light on the mechanism responsible for CP in the quark sector.

The DAQ Architecture comprises three functional blocks: front-end modules for the readout and digitization of the ~4000 channels in the KOTO detector; digital trigger modules with a dead timeless two-level design; and control plus fan-out electronics for the orchestration of the entire DAQ and final events readout. Figure 1 contains a block diagram of the DAQ Architecture for the KOTO detector.

The front-end electronics is spread over seventeen (17) 6U VME Crates, and includes three distinctive board flavours:

- Caesium Iodide (CsI) boards, using 14-Bit, 125 MHz ADC modules, each reading out 16 of ~3000 crystals in the KOTO CsI calorimeter.

- Veto Detector boards, using the same custom 14-Bit, 125MHz ADC Modules, fitted with a different firmware, for the readout of ~700 channels.

- Beam Hole Veto boards, using custom 12-Bit, 500MHz ADC Modules, with 4 channels per module, for the readout of up to 100 channels.

The Trigger electronics is designed to provide a dead timeless first level (L1) decision based on the total calorimeter energy and a second level (L2) trigger decision based on clustering and absence of signals in the veto detectors. Events passing the L2 trigger are stored in on-board memories for readout during accelerator spills.

The Trigger modules are housed in 9U VME crates with customized P3 backplane. The Trigger decision is made by the MAster Clock and TRigger Supervisor (MACTRIS) board, which generates and fans out control signals to the whole system, oversees the event readout and communicates with the Event Builder (EVB) and the accelerator.

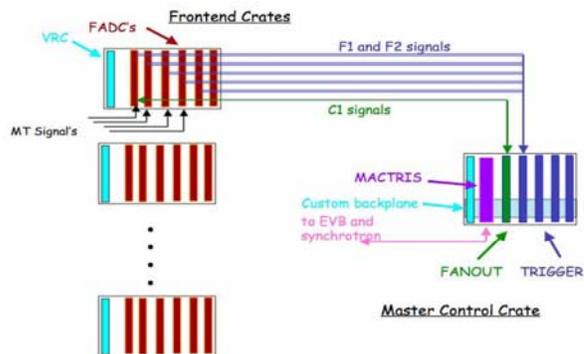


Figure 1: Block diagram of the DAQ Architecture for the KOTO detector.

II. TRIGGER DESIGN

The ADC boards receive the analog outputs of photomultipliers (PMT) attached to the frontend detectors. The analog pulses are shaped by 10-pole Gaussian low pass filters generating fixed-width Gaussian shaped pulses with a FWHM of about 45. By performing a fit to the output shape with a fixed width Gaussian one obtains two key parameters: the height of the Gaussian, which measures the total charge (energy) of the pulse, and the position of the peak, which measures its timing. Figure 2 shows the Gaussian output pulse shape for a sampling rate of 125 MHz.

The shaped pulses are saved inside a 4 μ s long pipeline where they wait for the L1 trigger decision. From the DAQ point of view, an event (i.e. the energy deposited by a single photon in the calorimeter) becomes a set of N consecutive samples centered around the L1 trigger. This is a variable

width signal enveloping the samples with total energy above a predetermined programmable threshold, as illustrated in Figure 2.

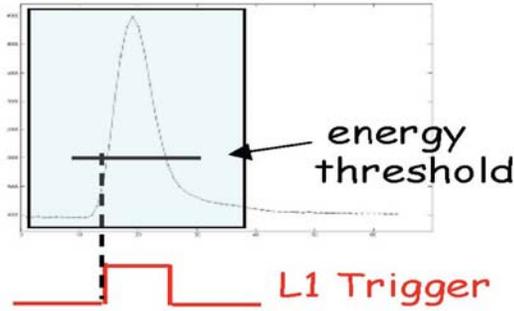


Figure 2: Shaped PMT pulse (black) and DAQ event (light blue) as a set of N consecutive samples around the L1 Trigger (red pulse).

The MACTRIS board aligns the L1 trigger decision with the PMT data as they exit the L1 pipeline and saves the events inside multiple L2 buffers, where each event can be fit to a gaussian template for a precise energy and timing measurement. The L2 Trigger decision is done asynchronously with the sampling clock but sequentially over each L2 buffer. The L2 trigger is based on clustering of adjacent CsI crystals to count photons in the calorimeter and on rejecting events with in-time activity in the veto counters.

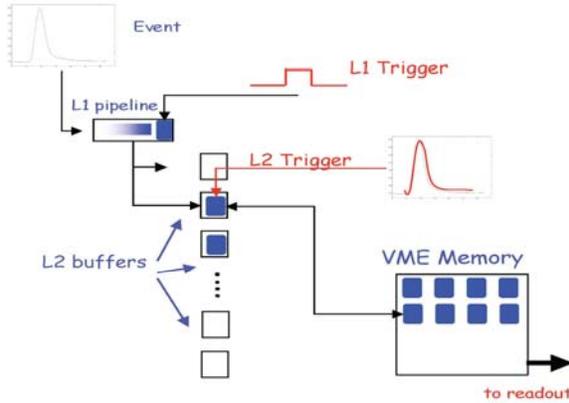


Figure 3: Cartoon view of the two-level Trigger for KOTO.

The two-level trigger allows a further reduction of readout rate to a manageable level. Events passing the L2 trigger are sent to an on-board VME Memory for readout via VME backplane. Figure 3 shows a cartoon of the two-level trigger design for KOTO.

III. FRONT-END MODULES

There are two different custom ADC Modules used in this experiment:

- 16-Channel, 14-BIT, 125MHz ADC Boards - for the CsI DAQ, and for the Veto Detector (with different firmware);
- 4-Channel, 12-BIT, 500MHz FADC Boards – for the Beam Hole Veto.

The ADC Boards are distributed over 17 VME Crates (6U). Each board connects directly to the Trigger Electronics via two Optical Links and one CAT5 cable.

Figure 4 presents the block diagram of one 14BIT, 125MHz 16-Channel ADC Board. The Boards are located 16 per one 6U VME Crate, and receive analog pulses directly from the PMTs. The Trigger Electronics connections are as follows:

- The CAT5 connection is used for the System Clock, and Trigger/Control Pulses.
- The Board Total Energy, is sent to the Trigger Modules via a 2.5Gbps Optical Link.
- The 2nd 2.5Gbps Optical Link is used for data readout upon a L1 Trigger pulse.

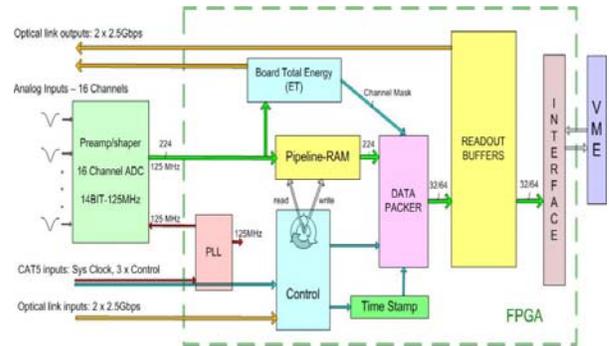


Figure 4: Block diagram of the 14-BIT, 125 MHz ADC Module.

In the CsI Calorimeter, every analog pulse generated by the photomultiplier tube is amplified and passed through a 10-pole filter/shaper with a cut-off frequency of about 10 MHz, which converts the fast PMT pulse into a Gaussian form, while keeping the total energy information constant. The filter/shaper was calculated for optimal Full Width Half-Height (FWHH) of the resulting pulse with respect to fitting and timing. Scope plots of the input and output signals are presented in Figure 5.

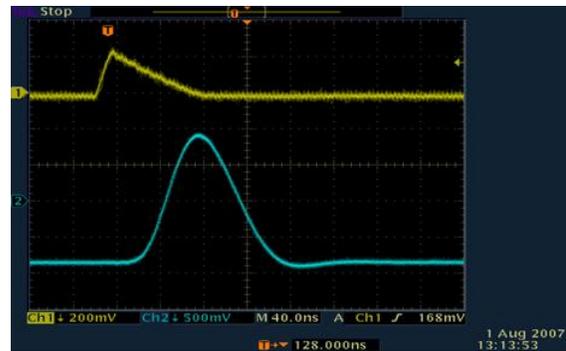


Figure 5: Scope plots of input and output signals through the shaper used in the KOTO CsI DAQ.

After shaping, each pulse is applied to a sample-and-hold ADC chip (AD9254).

Digitized data are processed locally with Field Programmable Gate Arrays (FPGAs), Altera EP2S60F1020C5 chips from the STRATIX II family [2] that perform the board total energy calculation and determine real-time board energy related values. These values are passed via 2.5Gbps Optical Links directly to the Trigger Electronics, for final decision, and eventual trigger pulse generation.

Each ADC module is provided with a pipeline, up to 4us (500 samples) long, which stores the acquisitions while awaiting the system trigger pulse. After a trigger, data are packed and buffered for readout. Data readout is performed via the 2nd front panel Optical Link.

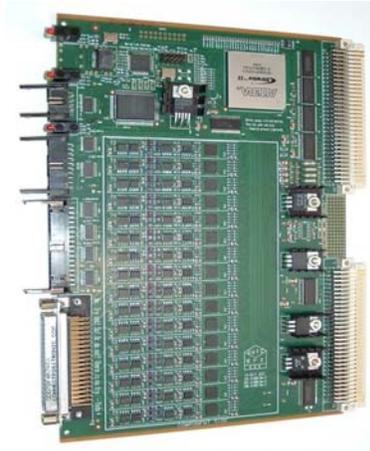


Figure 6: Prototype 14-Bit, 125 MHz ADC Module

A prototype 16-Channel, 14BIT, 125MHz ADC Board was built, and is presented in Figure 6. Preliminary tests showed an SNR of about 74dB.

The 4-Channel, 12-Bit, 500MHz Module, used in the Beam Hole Veto, has the block diagram presented in Figure 7. The functionality is similar to that of the 16-Channel CsI ADC Module. The FADC chips send LVDS signals to the FPGA, where a customized deserializer block reduces the bus frequency by a factor of four. Overall this 500MHz Module will process, and transmit the same volume of data as the 125MHz Board used for the CsI.

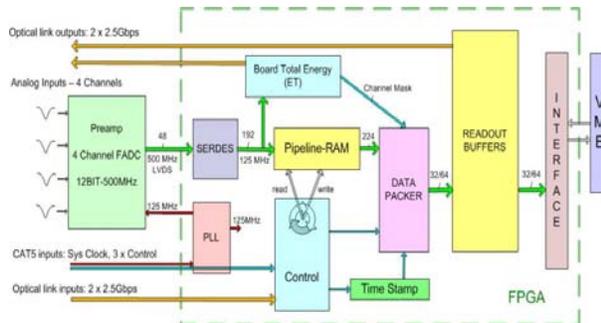


Figure 7: Block diagram of the 12-Bit, 500MHz FADC Module.

In the Beam Hole Veto FADC Module there are no shapers for the incoming analog signals. The PMT pulses are amplified and passed directly to the FADC chips.

Sampling for all calorimeter channels is simultaneous, on a low jitter System Clock.

IV. CONCLUSIONS

We presented the design of the DAQ for the KOTO detector at JPARC. The proposed architecture has three distinct functional blocks, one for the frontend readout, one for the trigger and one for DAQ controls.

The frontend electronics combines energy and time measurement in a single digitization step thanks to a new technique of waveform shaping. Its design is quite advanced and has already been tested in a 16 channel testbeam.

The digital trigger is designed to provide a deatimeless first level decision based on the total deposited energy and an asynchronous second level decision based on energy clustering and in-time veto signal rejection.

A commissioning run is scheduled for end of 2009, with Phase-1 data taking starting in winter 2010. The modularity in the KOTO DAQ design should provide enough flexibility to be able to cope with the increase in event rates expected for Phase-2 of the experiment.

V. REFERENCES

- [1] E14: Proposal for $K_L^0 \rightarrow \pi^0 \nu \bar{\nu}$ Experiment at JParc, approved July 2007.
- [2] Altera Corporation, Stratix II Device Handbook, v.2.1., May 2007.