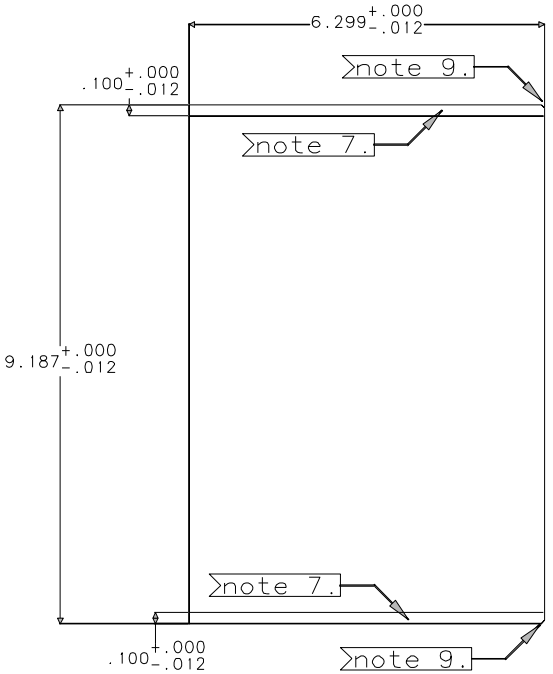

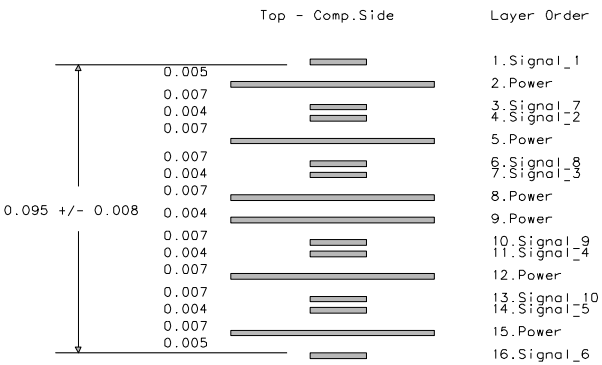

BOARD's DRILL SCHEDULE

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Tolerance	COMMENT
○	.014	4517	YES	---	
⊞	.015748031	144	YES	---	
⌀	.0236	114	YES	Note 12.	Note 12.
⊟	.035	1	YES	---	
⊖	.037	9	YES	---	
◫	.041	557	YES	---	
⊕	.042	40	YES	---	
□	.057	18	YES	---	
	.062	2	YES	---	
	.106	6	NO	---	
	.125	2	YES	---	

Board Characteristics

0. All dimensions are given in inches unless specified otherwise.
1. Material FR4 with Tg>170C, E.g. FR406
2. Minimum trace width and clearence: 0.006" on Signal_1,6 (Top and Bottom);
3. Minimum trace width and clearence: 0.005" on Signal_2,3,4,5 (all stripline traces);
4. 1 oz copper for all power layers and for Signal_1,2 (Top and Bottom)
   1/2 oz copper for Stripline trace layers (Signal_2,3,4,5).
5. Immersion Gold over copper, with min. Ni: 2.5-5 um; Au: 0.05-0.2 um.
   Apply Solder Mask over bare copper.
6. Board Thickness: 0.093 +/- 0.008
7. Mill the Top and Bottom of board on the solder side to a thickness of 0.063" +/- 0.008
8. Silkscreen on Component and Solder Sides.
9. 45 degree chamfer.
10. FHS tolerances: +/- 0.002 unless specified otherwise.
11. Interlayer spacing as specified
12. This is a pressfit technology thru hole with the following specs:
    12-1. Finished plated hole size: 0.59 - 0.65 mm.
    12-2. Drilled hole size: 0.7mm +/- 0.02mm
    12-3. Min. Thickness of thru hole plating: Cu: 25 μm; Ni: 2.5-5 μm; Au: 0.05-0.2 μm.
13. Zc=55 Ohm +/- 5 Ohm for 0.005" stripline and 0.006" microstrip traces on all layers.
    Perform TDR test for all signal layers.
    Present TDR test results for all signal layers.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX
.XXX
DO NOT SCALE DRAWING

TREATMENT

FINISH

SIMILAR TO | ACT. WT | CALC WT

CONTRACT NO.

APPROVALS	DATE
DRAWN M.Bogdan	6/12/07
CHECKED M.Bogdan	6/12/07
ISSUED	

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE: 14-BIT ADC Board Specification Drawing

SIZE B | FSCM NO. | DWG. NO. A - 2606 | REV. A

SCALE 1/2 | SHEET

THIS SHEET IS COMPUTER GENERATED