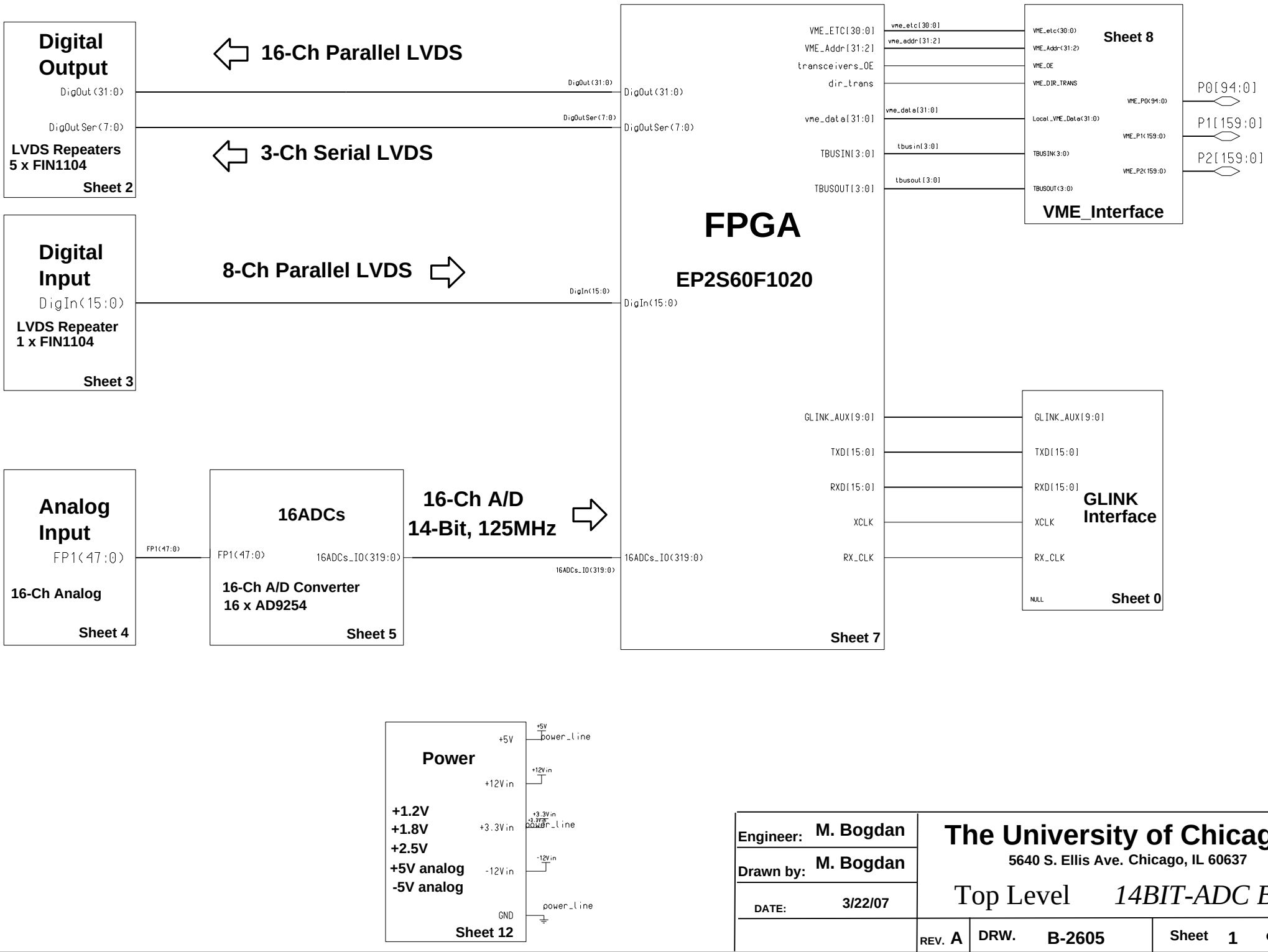
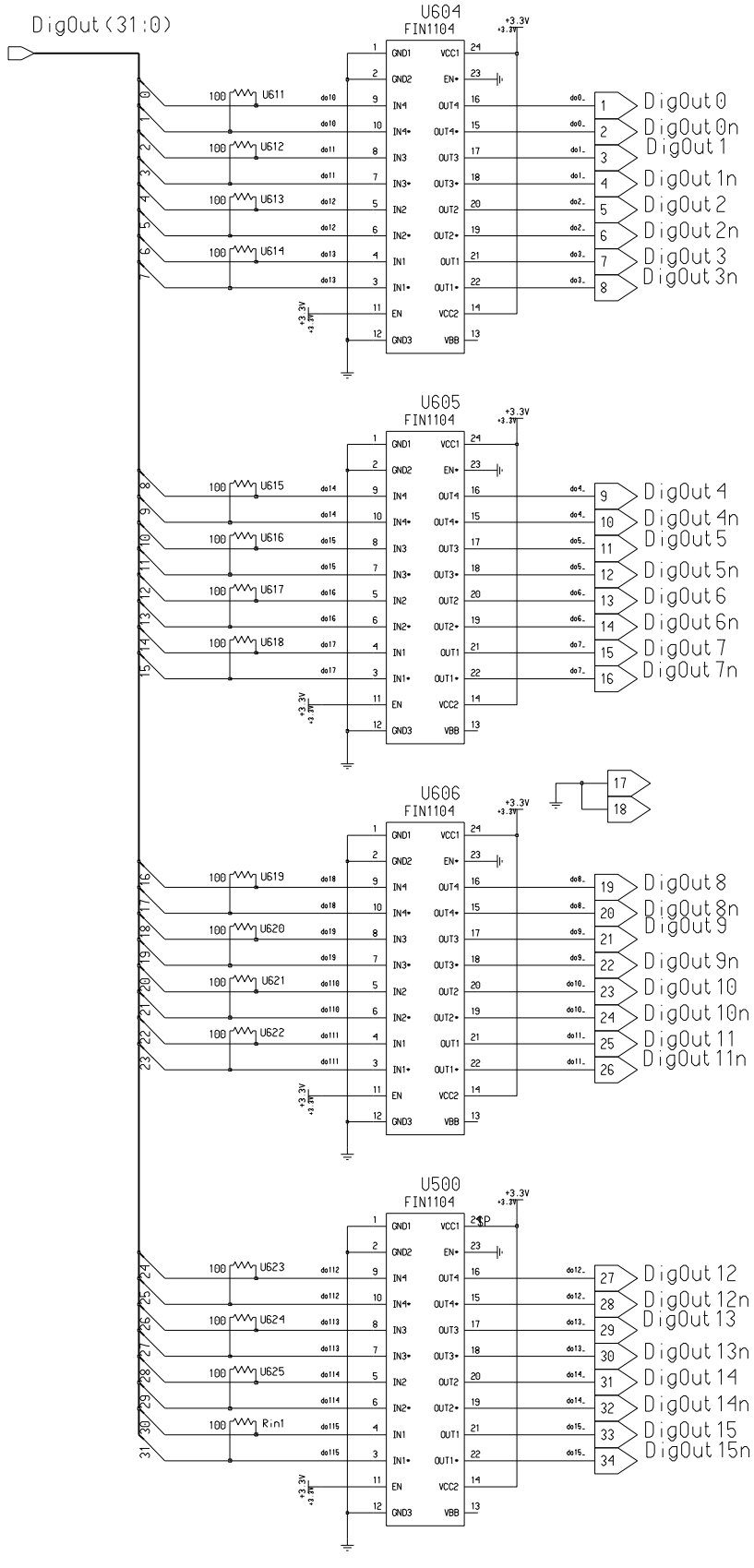


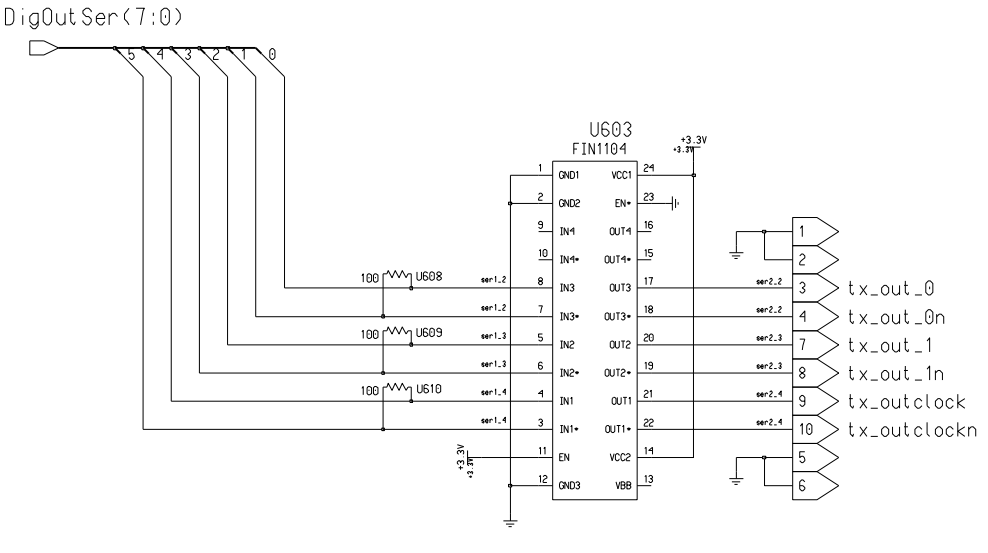
Engineer: M. Bogdan	**The University of Chicago**		
Drawn by: M. Bogdan	5640 S. Ellis Ave. Chicago, IL 60637		
DATE: 3/22/07	Top Level *14BIT-ADC Board*		
	REV. A	DRW. B-2605	Sheet 1 of 12

LVDS paralel output

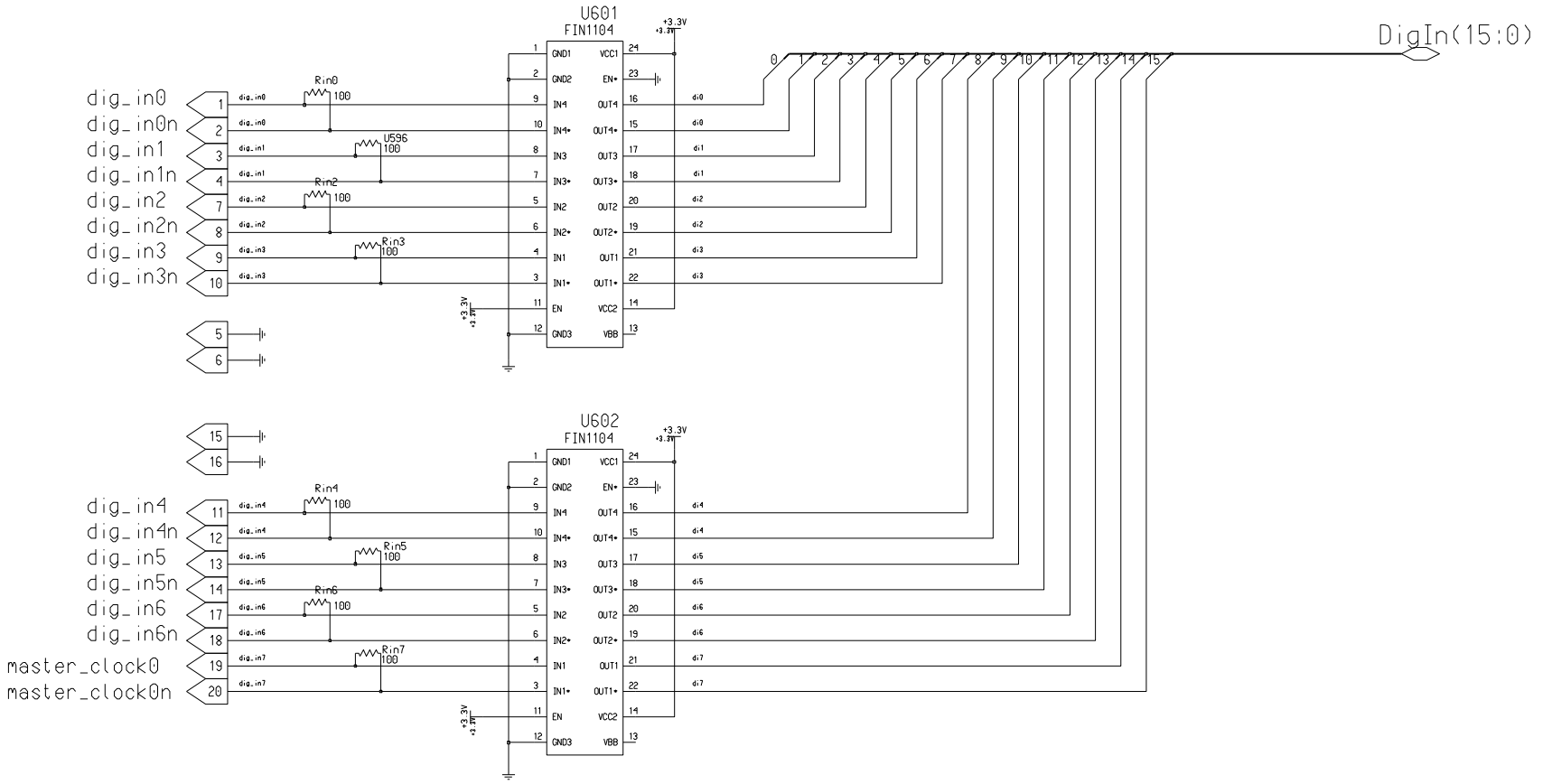


LVDS serial output

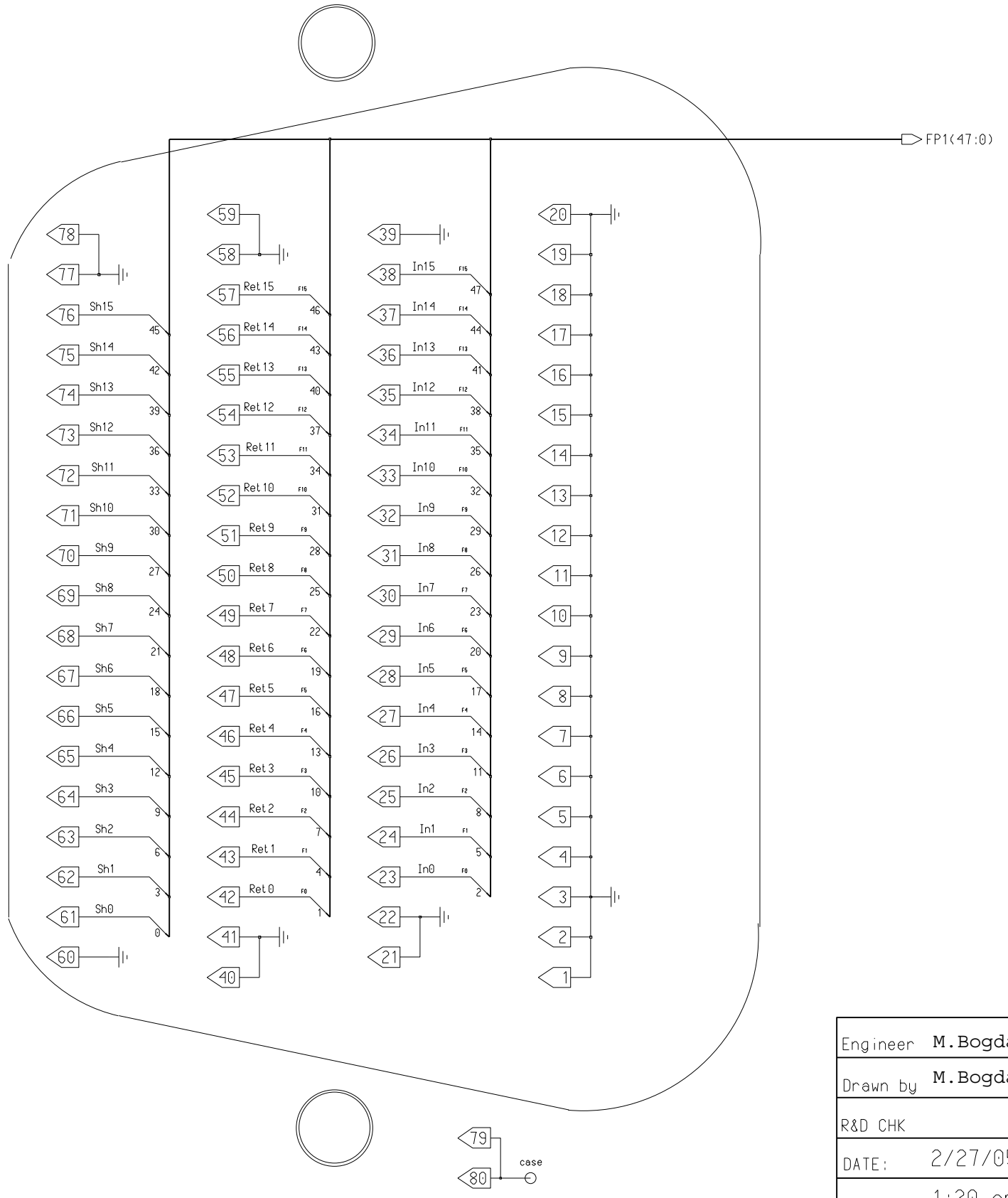
Insert transceiver here:



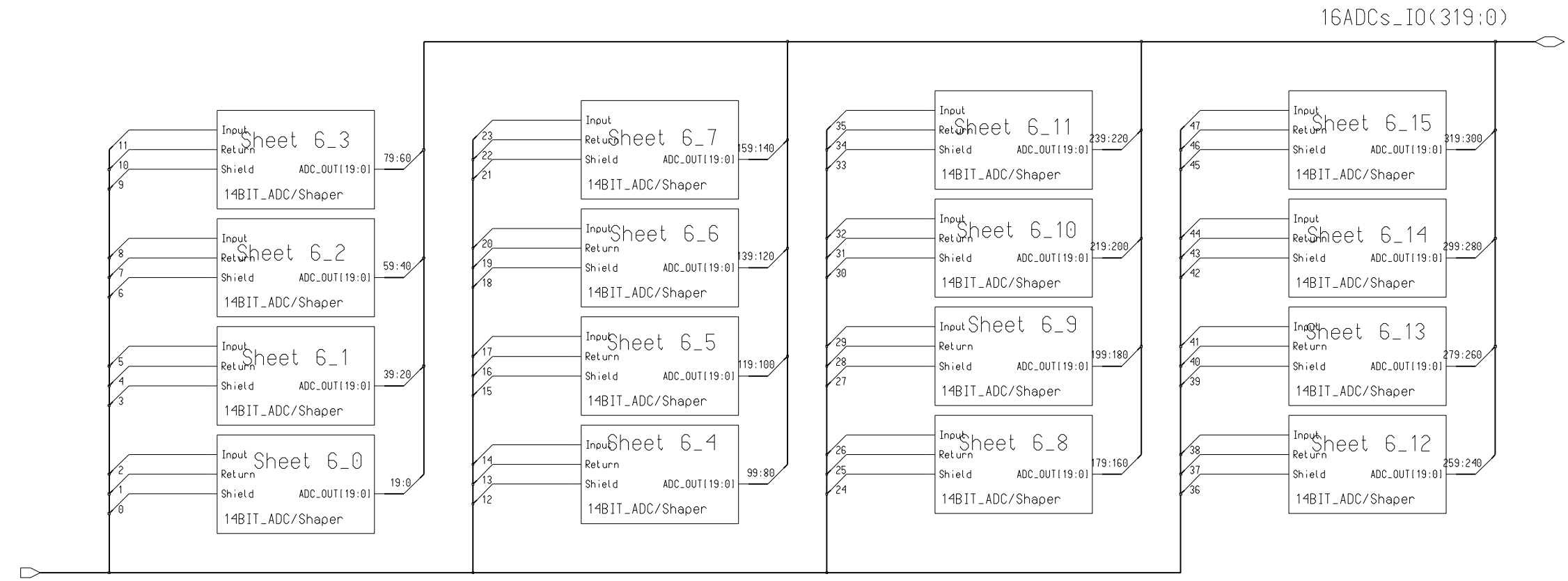
Engineer M.Bogdan	The University of Chicago 5640 S. Ellis Ave. Chicago, IL 60637	
Drawn by M.Bogdan		
R&D CHK	TITLE	Size C
DATE: 3/15/05	**Front Panel - digital output** *JPARC-K 14BIT-ADC Board*	
TIME: 1:30 pm		
QA CHK	REV A	DRW. B-2605 Sheet 2 of 12



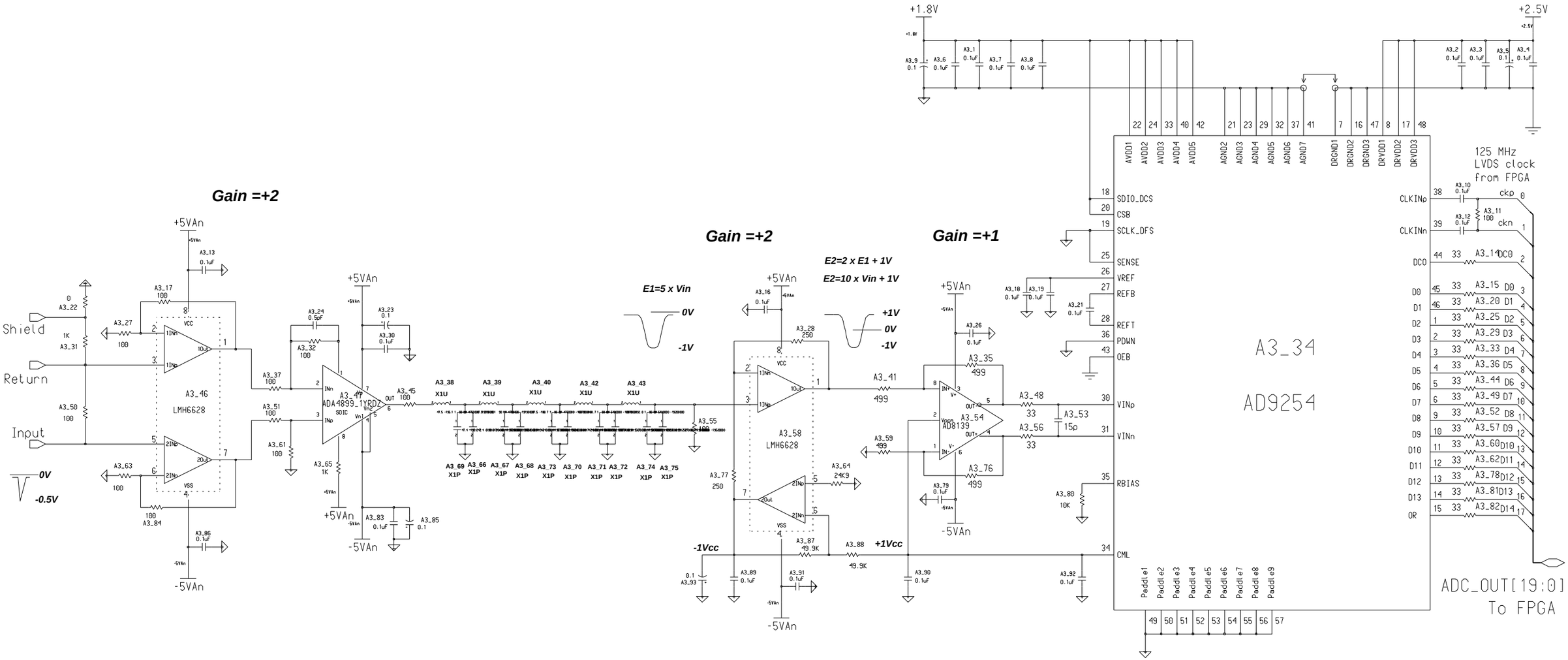
Engineer	M.Bogdan	The University of Chicago 5640 S. Ellis Ave. Chicago, IL 60637	
Drawn by	M.Bogdan		
R&D CHK		TITLE	Size C
DATE:	3/15/07	**Front Panel - digital input** *JPARC-K 14BIT-ADC Board*	
TIME:	1:30 pm		
QA CHK		REV A	DRW. B-2605 — Sheet 3 of 12



Engineer M.Bogdan	The University of Chicago 5640 S. Ellis Ave. Chicago, IL 60637
Drawn by M.Bogdan	
R&D CHK	TITLE: Front Panel -analog input *JPARC-K 14BIT-ADC Board*
DATE: 2/27/05	Size C
TIME: 1:30 pm	
QA CHK	REV A · DRW. B-2605 · Sheet 4 of 12



Engineer	M.Bogdan	The University of Chicago 5640 S. Ellis Ave. Chicago, IL 60637	
Drawn by	M.Bogdan		
R&D CHK		TITLE ADC Channels 0 - 15 *JPARC-K 14BIT-ADC Board*	Size C
DATE:	1/12/07		
TIME:	2:00 pm		
QA CHK		REV A	DRW. B-2605 Sheet 5 of 12



Notes:

In = 0V -> E1=0V -> E2=+1V -> 11 1111 1111 1111

In = -0.5V -> E1=-1V -> E2=-1V -> 00 0000 0000 0000

There are 16 channels on one board.

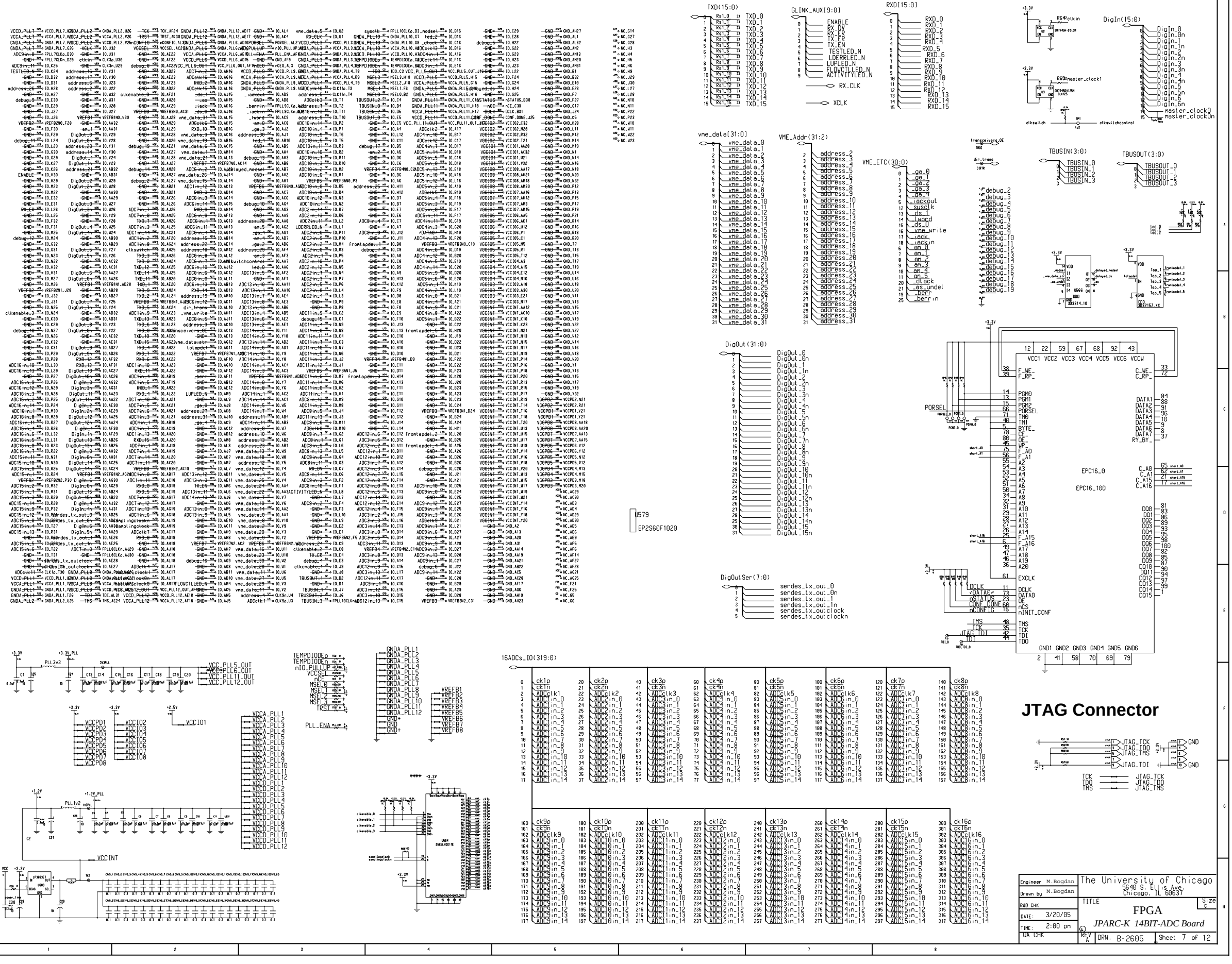
AD9254 receives LVDS clock from the FPGA.

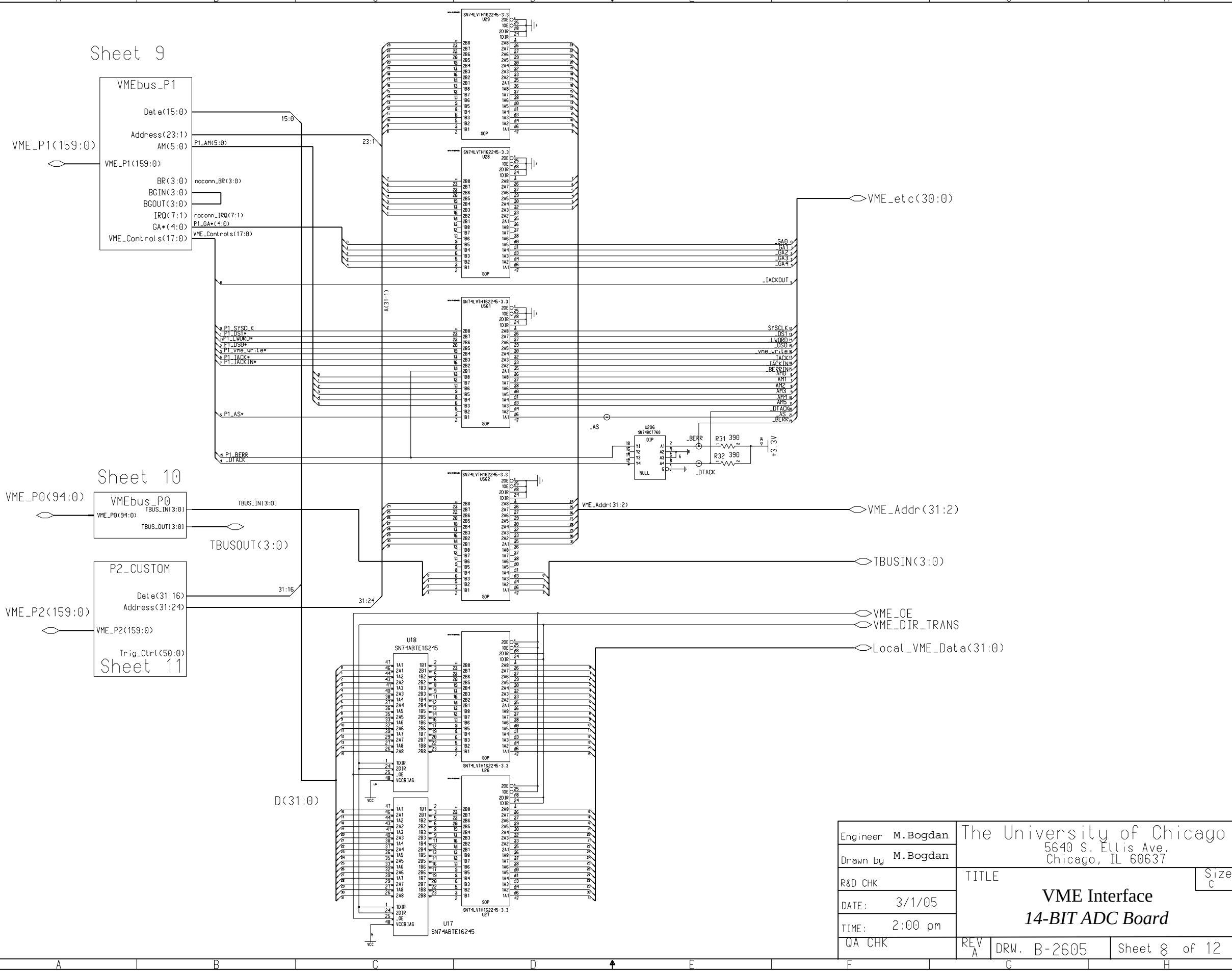
AD9254 sends 14-BIT data bus and clock to FPGA.

All 0.1uF caps are Panasonic ECJ-1VB1C104K - 0603.

All 33 Ohm resistors are 0402; All other resistors are 0603.

Engineer M.Bogdan		
Drawn by M.Bogdan		
R&D CHK	TITLE	Size C
DATE: 4/12/07	ADC Channel j	
TIME: 11:00 am		
QA CHK	REV A	DRW. B-2605 Sheet 6_j of 12


TXD(15:0)
TXD_0
TXD_1
TXD_2
TXD_3
TXD_4
TXD_5
TXD_6
TXD_7
TXD_8
TXD_9
TXD_10
TXD_11
TXD_12
TXD_13
TXD_14
TXD_15
GLINK_AUX[9:0]
ENABLE
RX_DV
RX_ER
TX_ER
TX_EN
TESTLED_N
LDERRLED_N
LUPLED_N
FLOWCTLLED_N
ACTIVITYLED_N
RX_CLK
XCLK
RXD[15:0]
RXD_0
RXD_1
RXD_2
RXD_3
RXD_4
RXD_5
RXD_6
RXD_7
RXD_8
RXD_9
RXD_10
RXD_11
RXD_12
RXD_13
RXD_14
RXD_15
DigIn(15:0)
DigIn_0
DigIn_0n
DigIn_1
DigIn_1n
DigIn_2
DigIn_2n
DigIn_3
DigIn_3n
DigIn_4
DigIn_4n
DigIn_5
DigIn_5n
DigIn_6
DigIn_6n
master_clock0
master_clock0n
clkswitch
clkswitchcontrol
vme_data[31:0]
vme_data_0
vme_data_1
vme_data_2
vme_data_3
vme_data_4
vme_data_5
vme_data_6
vme_data_7
vme_data_8
vme_data_9
vme_data_10
vme_data_11
vme_data_12
vme_data_13
vme_data_14
vme_data_15
vme_data_16
vme_data_17
vme_data_18
vme_data_19
vme_data_20
vme_data_21
vme_data_22
vme_data_23
vme_data_24
vme_data_25
vme_data_26
vme_data_27
vme_data_28
vme_data_29
vme_data_30
vme_data_31
VME_Addr(31:2)
address_2
address_3
address_4
address_5
address_6
address_7
address_8
address_9
address_10
address_11
address_12
address_13
address_14
address_15
address_16
address_17
address_18
address_19
address_20
address_21
address_22
address_23
address_24
address_25
address_26
address_27
address_28
address_29
address_30
address_31
VME_ETC(30:0)
_ga_0
_ga_1
_ga_2
_ga_3
_ga_4
_wackout
_suscLk
_ds_1
_Lword
_ds_0
_vme_write
_iack
_iackin
_am_0
_am_1
_am_2
_am_3
_am_4
_am_5
_dtack
_as_undel
_berr
_berrin
transceivers_OE
TRXE
dir_trans
DIR1B
debug_2
debug_3
debug_4
debug_5
debug_6
debug_7
debug_8
debug_9
debug_10
debug_11
debug_12
debug_13
debug_14
debug_15
debug_16
debug_17
debug_18
debug_19
TBUSIN(3:0)
TBUSIN_0
TBUSIN_1
TBUSIN_2
TBUSIN_3
TBUSOUT(3:0)
TBUSOUT_0
TBUSOUT_1
TBUSOUT_2
TBUSOUT_3
DigOut(31:0)
DigOut_0
DigOut_0n
DigOut_1
DigOut_1n
DigOut_2
DigOut_2n
DigOut_3
DigOut_3n
DigOut_4
DigOut_4n
DigOut_5
DigOut_5n
DigOut_6
DigOut_6n
DigOut_7
DigOut_7n
DigOut_8
DigOut_8n
DigOut_9
DigOut_9n
DigOut_10
DigOut_10n
DigOut_11
DigOut_11n
DigOut_12
DigOut_12n
DigOut_13
DigOut_13n
DigOut_14
DigOut_14n
DigOut_15
DigOut_15n
DigOutSer(7:0)
serdes_tx_out_0
serdes_tx_out_0n
serdes_tx_out_1
serdes_tx_out_1n
serdes_tx_outclock
serdes_tx_outclockn
U579
EP2S60F1020
EPC16_0
EPC16_100
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DATA0
DATA1
DATA2
DATA3
DATA4
DATA5
DATA6
DATA7
F_WE_
F_RP_
F_A0
F_A1
F_A15
F_A16
C_WE_
C_RP_
C_A0
C_A1
C_A15
C_A16
PGM0
PGM1
PGM2
PORSEL
TM0
TM1
BYTE_
CE_
OE_
WP_
RY_BY_
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
EXCLK
DCLK
DATA0
nSTATUS
CONF_DONE
nCONFIG
nINIT_CONF
TMS
TCK
TDI
TDO
GND1 GND2 GND3 GND4 GND5 GND6
JTAG Connector
JTAG_TCK
JTAG_TDO
JTAG_TMS
JTAG_TDI
GND
TCK
TDO
TMS
16ADCs_IO(319:0)
PLL_ENA
TEMPDIODEp
TEMPDIODEn
nIO_PULLUP
VCCSEL
nCE
MSEL0
MSEL1
MSEL2
MSEL3
TRST
VREFB1
VREFB2
VREFB3
VREFB4
VREFB5
VREFB6
VREFB7
VREFB8
VCCA_PLL1
VCCA_PLL2
VCCA_PLL3
VCCA_PLL4
VCCA_PLL5
VCCA_PLL6
VCCA_PLL7
VCCA_PLL8
VCCA_PLL9
VCCA_PLL10
VCCA_PLL11
VCCA_PLL12
VCCD_PLL1
VCCD_PLL2
VCCD_PLL3
VCCD_PLL4
VCCD_PLL5
VCCD_PLL6
VCCD_PLL7
VCCD_PLL8
VCCD_PLL9
VCCD_PLL10
VCCD_PLL11
VCCD_PLL12
VCCPD1
VCCPD2
VCCPD3
VCCPD4
VCCPD5
VCCPD6
VCCPD7
VCCPD8
VCCIO1
VCCIO2
VCCIO3
VCCIO4
VCCIO5
VCCIO6
VCCIO7
VCCIO8
VCCINT
PLL3v3
PLL1v2
VCC_PLL5_OUT
VCC_PLL6_OUT
VCC_PLL11_OUT
VCC_PLL12_OUT
GNDA_PLL1
GNDA_PLL2
GNDA_PLL3
GNDA_PLL4
GNDA_PLL5
GNDA_PLL6
GNDA_PLL7
GNDA_PLL8
GNDA_PLL9
GNDA_PLL10
GNDA_PLL11
GNDA_PLL12
GND*
GND
GND+
Engineer M.Bogdan
Drawn by M.Bogdan
R&D CHK
DATE: 3/20/05
TIME: 2:00 pm
QA CHK
The University of Chicago
5640 S. Ellis Ave.
Chicago, IL 60637
TITLE
FPGA
JPARC-K 14BIT-ADC Board
Size C
REV A
DRW. B-2605
Sheet 7 of 12



Engineer M.Bogdan	The University of Chicago 5640 S. Ellis Ave. Chicago, IL 60637	
Drawn by M.Bogdan		
R&D CHK	TITLE	Size C
DATE: 3/1/05	VME Interface *14-BIT ADC Board*	
TIME: 2:00 pm		
QA CHK	REV A / DRW. B-2605	Sheet 8 of 12

P1

VME_P1(159:0)

BGIN(3:0)
BGOUT(3:0)
BR(3:0)
VME_Controls(17:0)
GA*(4:0)
IRQ(7:1)
AM(5:0)
Address(23:1)
Data(15:0)

TM0 Z1 129	D0 A1 1	BBSY* B1 33	D8 C1 65
ground Z2 130	D1 A2 2	BCLR* B2 34	D9 C2 66
TM1 Z3 131	D2 A3 3	ACFAIL* B3 35	D10 C3 67
ground Z4 132	D3 A4 4	BG0IN* B4 36	D11 C4 68
TM2 Z5 133	D4 A5 5	BG0OUT* B5 37	D12 C5 69
ground Z6 134	D5 A6 6	BG1IN* B6 38	D13 C6 70
TM3 Z7 135	D6 A7 7	BG1OUT* B7 39	D14 C7 71
ground Z8 136	D7 A8 8	BG2IN* B8 40	D15 C8 72
TM4 Z9 137	ground A9 9	BG2OUT* B9 41	ground C9 73
ground Z10 138	SYSCLK A10 10	BG3IN* B10 42	SYSFAIL* C10 74
RTRY* Z11 139	ground A11 11	BG3OUT* B11 43	BERR* C11 75
ground Z12 140	DS1* A12 12	BR0* B12 44	SYSRESET* C12 76
ReservedBus0 Z13 141	DS0* A13 13	BR1* B13 45	LWORD* C13 77
ground Z14 142	WRITE* A14 14	BR2* B14 46	AM5 C14 78
ReservedBus1 Z15 143	ground A15 15	BR3* B15 47	A23 C15 79
ground Z16 144	DTACK* A16 16	AM0 B16 48	A22 C16 80
ReservedBus2 Z17 145	ground A17 17	AM1 B17 49	A21 C17 81
ground Z18 146	AS* A18 18	AM2 B18 50	A20 C18 82
ReservedBus3 Z19 147	ground A19 19	AM3 B19 51	A19 C19 83
ground Z20 148	IACK* A20 20	ground B20 52	A18 C20 84
ReservedBus4 Z21 149	IACKIN* A21 21	SERCLK B21 53	A17 C21 85
ground Z22 150	IACKOUT* A22 22	SERDAT* B22 54	A16 C22 86
ReservedBus5 Z23 151	AM4 A23 23	ground B23 55	A15 C23 87
ground Z24 152	A7 A24 24	IRQ7* B24 56	A14 C24 88
ReservedBus6 Z25 153	A6 A25 25	IRQ6* B25 57	A13 C25 89
ground Z26 154	A5 A26 26	IRQ5* B26 58	A12 C26 90
ReservedBus7 Z27 155	A4 A27 27	IRQ4* B27 59	A11 C27 91
ground Z28 156	A3 A28 28	IRQ3* B28 60	A10 C28 92
SBB Z29 157	A2 A29 29	IRQ2* B29 61	A9 C29 93
ground Z30 158	A1 A30 30	IRQ1* B30 62	A8 C30 94
SBA Z31 159	-12V A31 31	+5V_STDBY B31 63	+12V C31 95
ground Z32 160	+5V A32 32	+5V B32 64	+5V C32 96

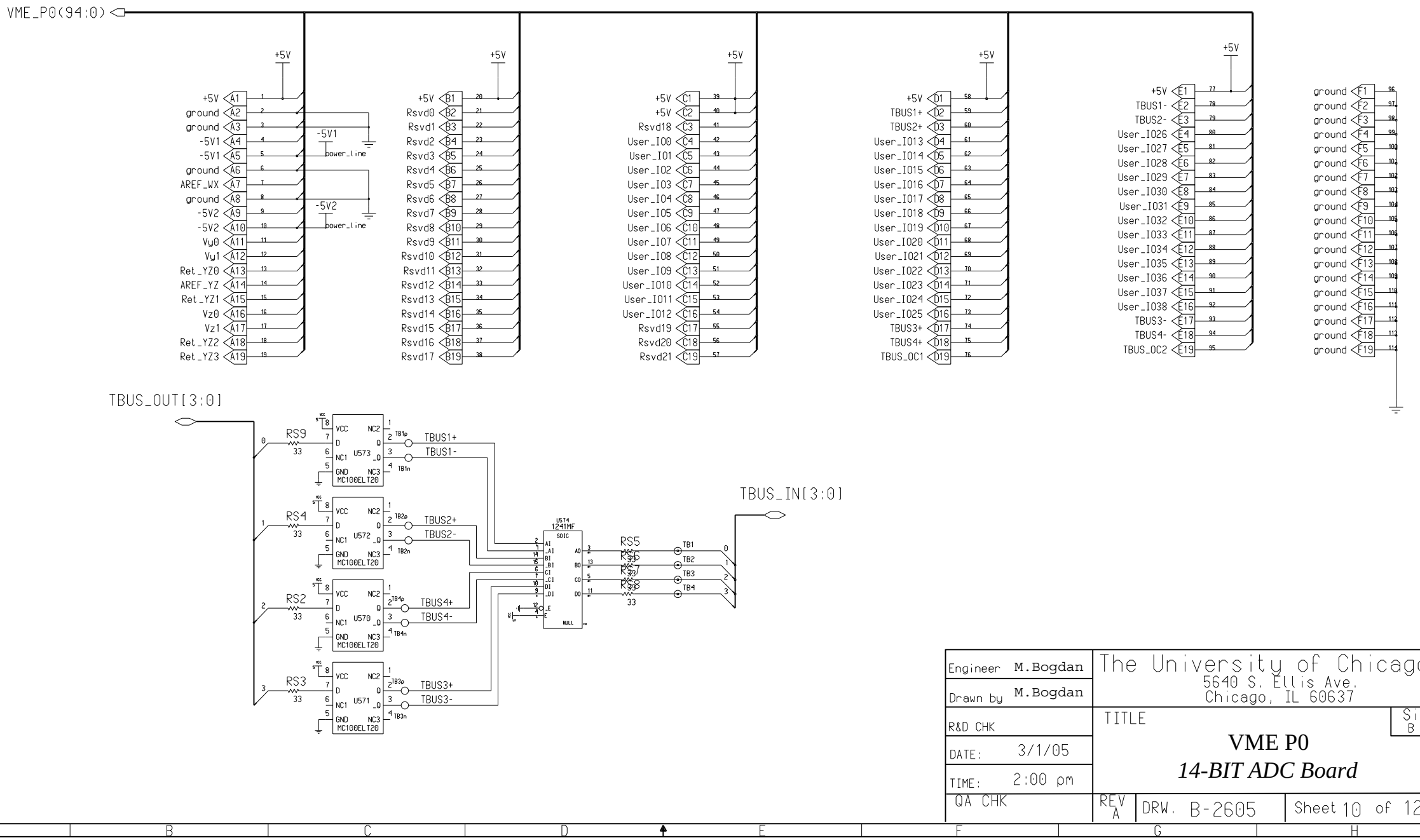
VPC D1 97	
ground D2 98	
+V1 D3 99	
+V2 D4 100	
ReservedU0 D5 101	
-V1 D6 102	
-V2 D7 103	
ReservedU1 D8 104	
GAP* D9 105	
GA0* D10 106	
GA1* D11 107	
+3.3Vin D12 108	
GA2* D13 109	
+3.3Vin D14 110	
GA3* D15 111	
+3.3Vin D16 112	
GA4* D17 113	
+3.3Vin D18 114	
ReservedBus8 D19 115	
+3.3Vin D20 116	
ReservedBus9 D21 117	
+3.3Vin D22 118	
ReservedBus10 D23 119	
+3.3Vin D24 120	
ReservedBus11 D25 121	
+3.3Vin D26 122	
LII* D27 123	
+3.3Vin D28 124	
LIO* D29 125	
+3.3Vin D30 126	
ground D31 127	
VPC D32 128	

VCC
R1 2.5K R2 2K R3 2K R4 2K R5 2K
1K 1K 1K 1K 1K

-12Vin
+5V_STDBY
+12Vin
+5V
+3.3Vin

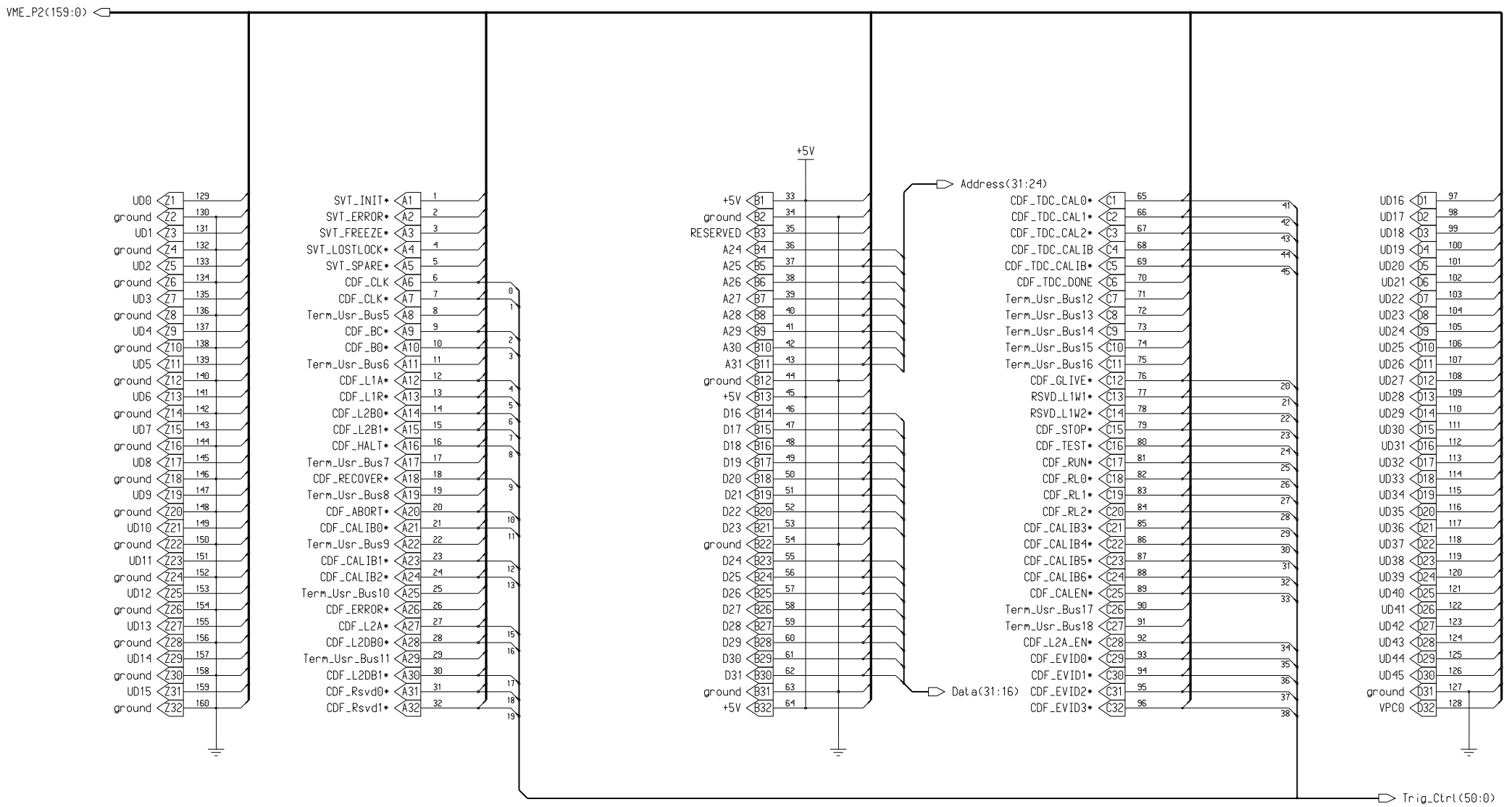
Engineer	M.Bogdan	The University of Chicago 5640 S. Ellis Ave. Chicago, IL 60637	
Drawn by	M.Bogdan		
R&D CHK		TITLE	Size C
DATE:	3/1/05	VME-P1 *14-BIT ADC Board*	
TIME:	2:00 pm		
QA CHK		REV A	DRW. B-2605 Sheet 9 of 12

P0

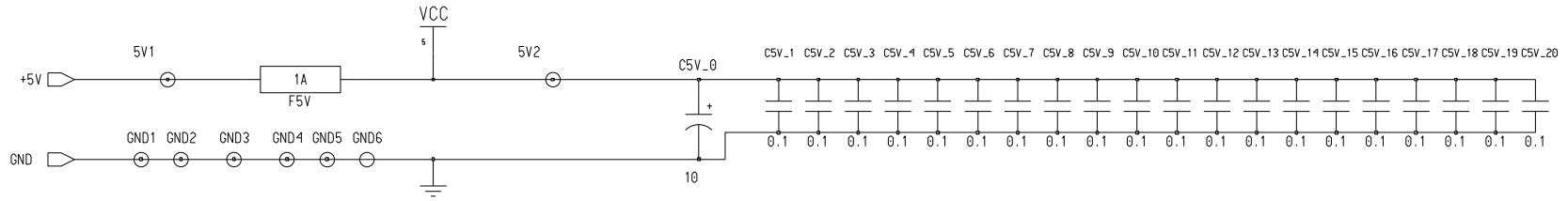


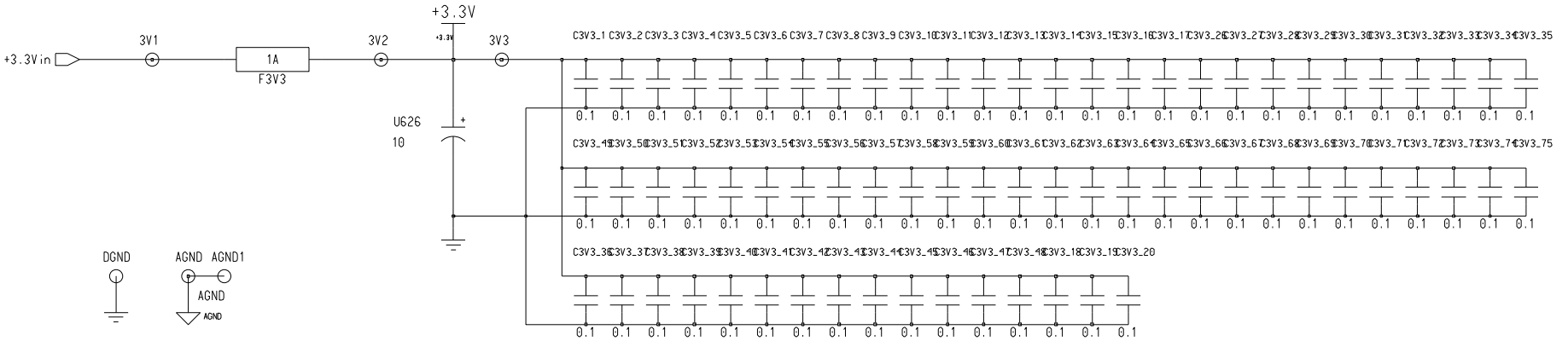
Engineer M.Bogdan	The University of Chicago 5640 S. Ellis Ave. Chicago, IL 60637	
Drawn by M.Bogdan		
R&D CHK	TITLE	Size B
DATE: 3/1/05	VME P0 *14-BIT ADC Board*	
TIME: 2:00 pm		
QA CHK	REV A / DRW. B-2605	Sheet 10 of 12

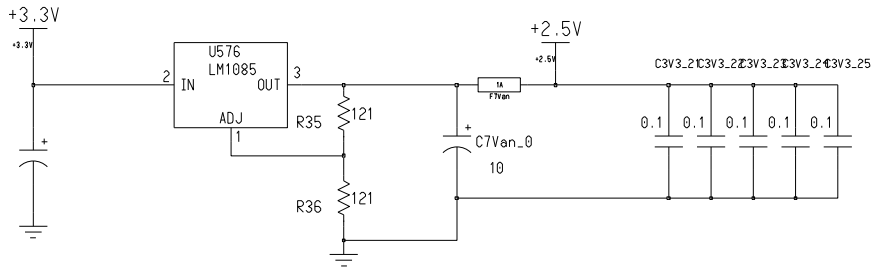
P2

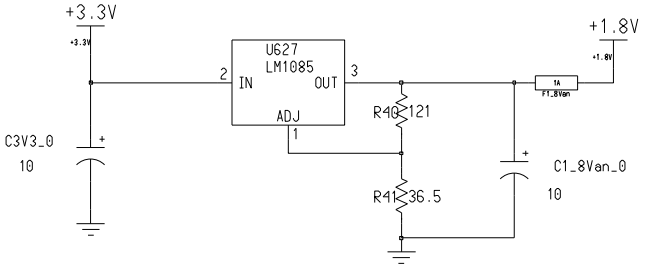


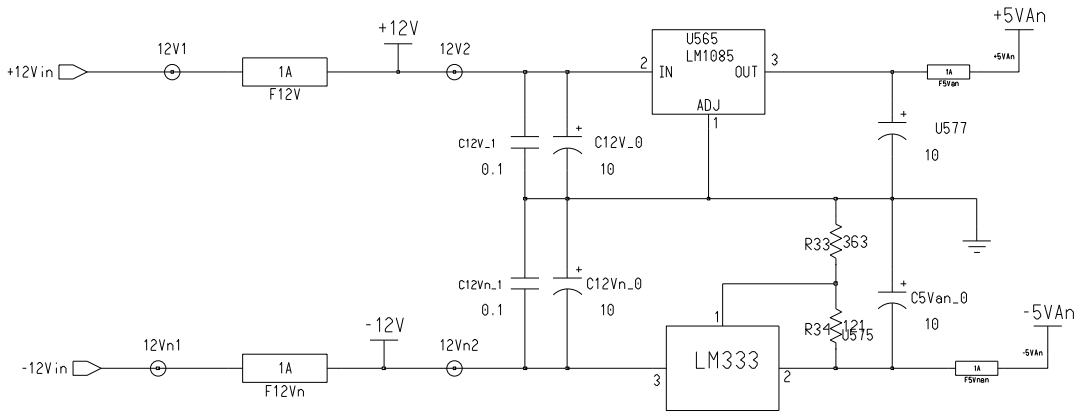
Engineer M.Bogdan	The University of Chicago 5640 S. Ellis Ave. Chicago, IL 60637	
Drawn by M.Bogdan		
R&D CHK	TITLE	Size B
DATE: 3/1/05	VME-P2 *14-BIT ADC Board*	
TIME: 2:00 pm		
QA CHK	REV A | DRW. B-2605	Sheet 11 of 12



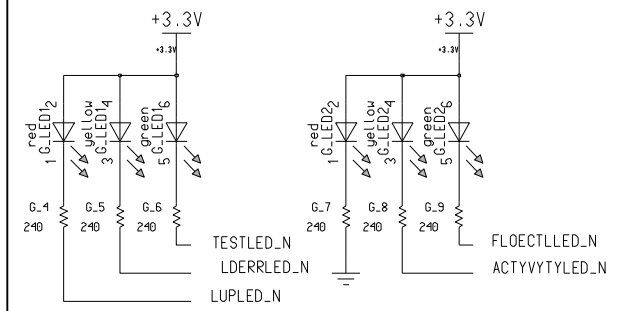


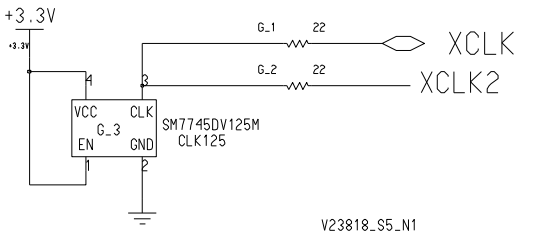


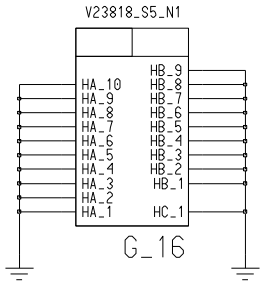


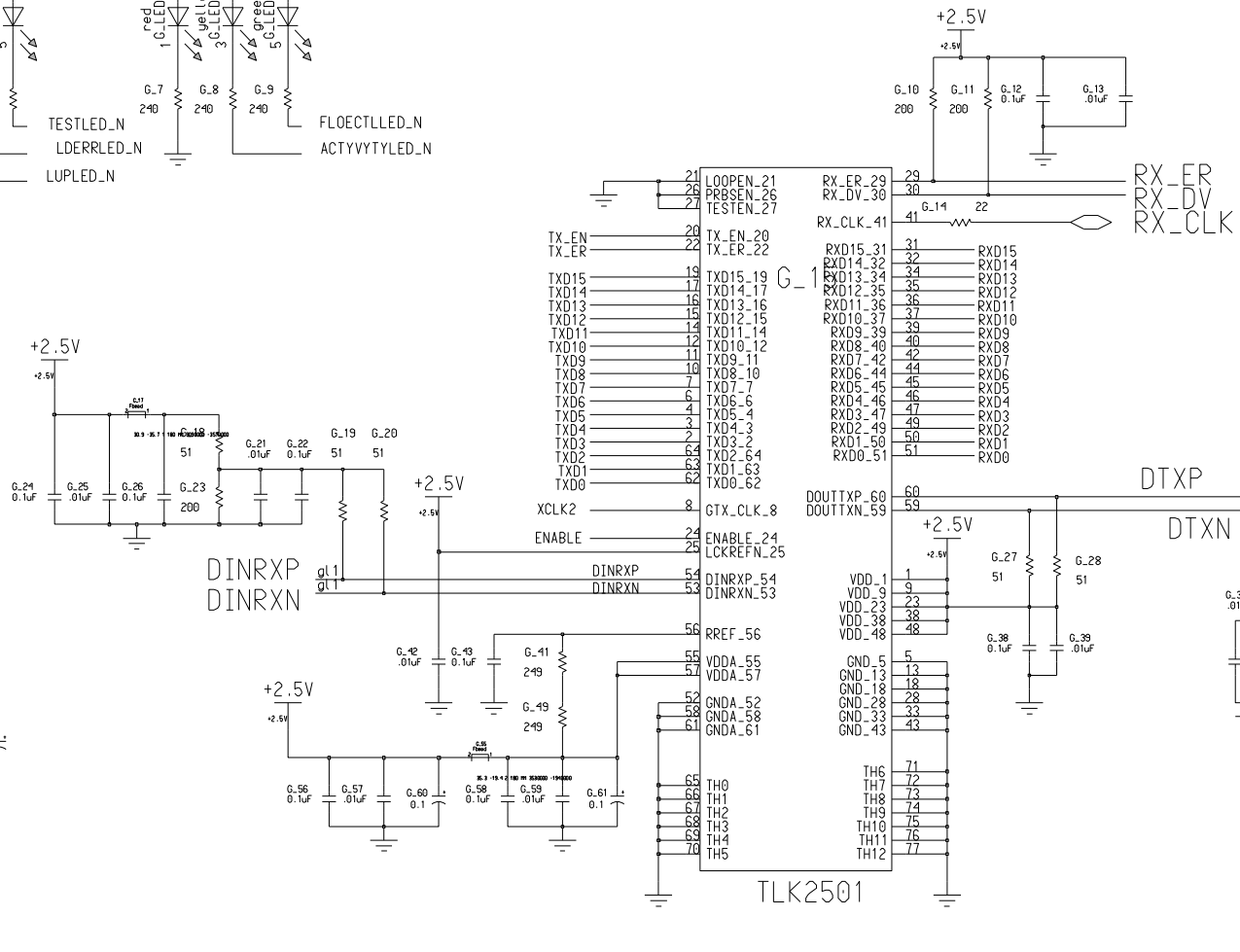


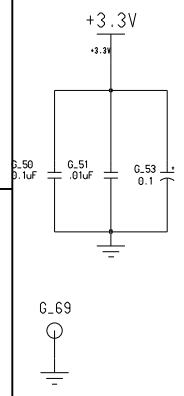
Engineer M.Bogdan	The University of Chicago 5640 S. Ellis Ave. Chicago, IL 60637	
Drawn by M.Bogdan		
R&D CHK	TITLE	Size B
DATE: 3/7/05	**Power** ***14BIT-ADC Board***	
TIME: 2:00 pm		
QA CHK	REV A | DRW. B-2605	Sheet 12 of 12

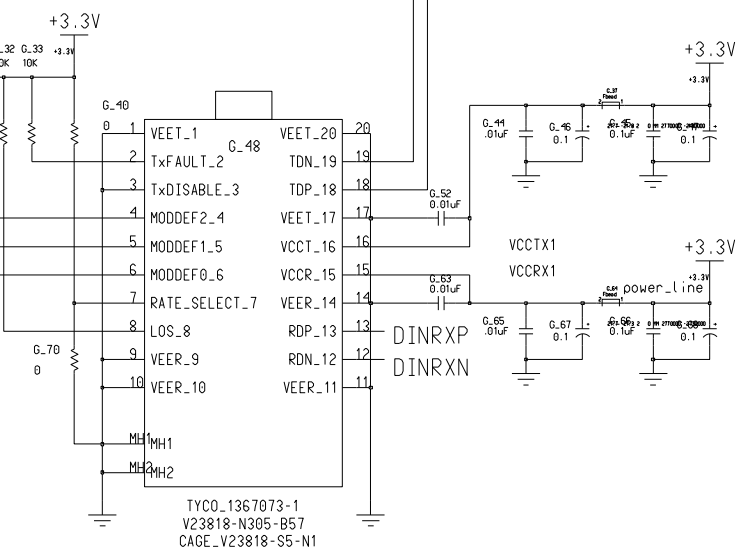


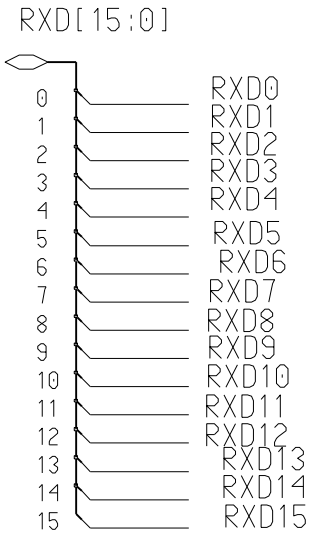


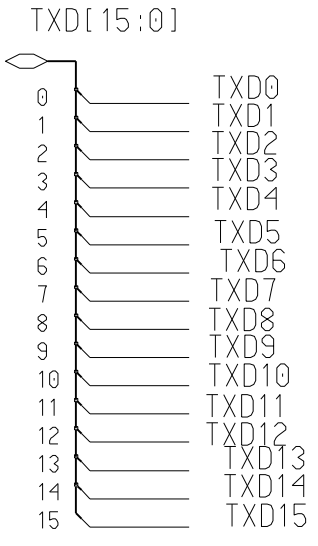


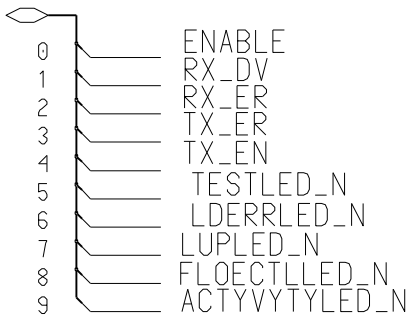












Engineer	M.Bogdan	The University of Chicago 5640 S. Ellis Ave. Chicago, IL 60637
Drawn by	M.Bogdan	
R&D CHK		TITLE Optical Link Block *14-BIT ADC Board*
DATE:	4/16/05	Size B
TIME:	2:00 pm	
QA CHK		REV A | DRW. B-2605 | Sheet 0 of 12