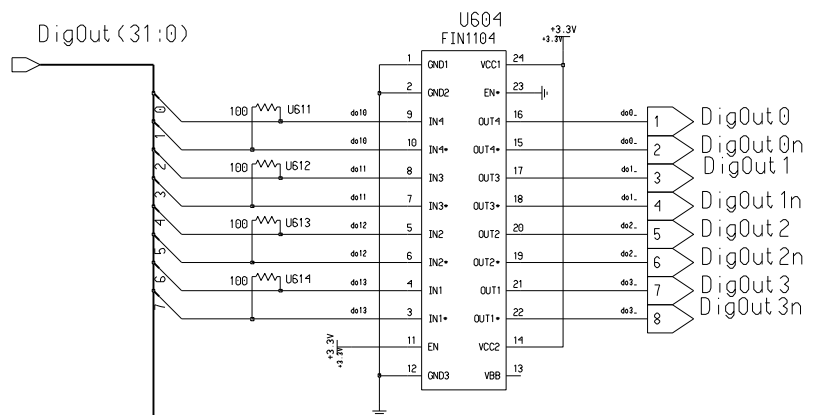


### LVDS parallel output

DigOut (31:0)

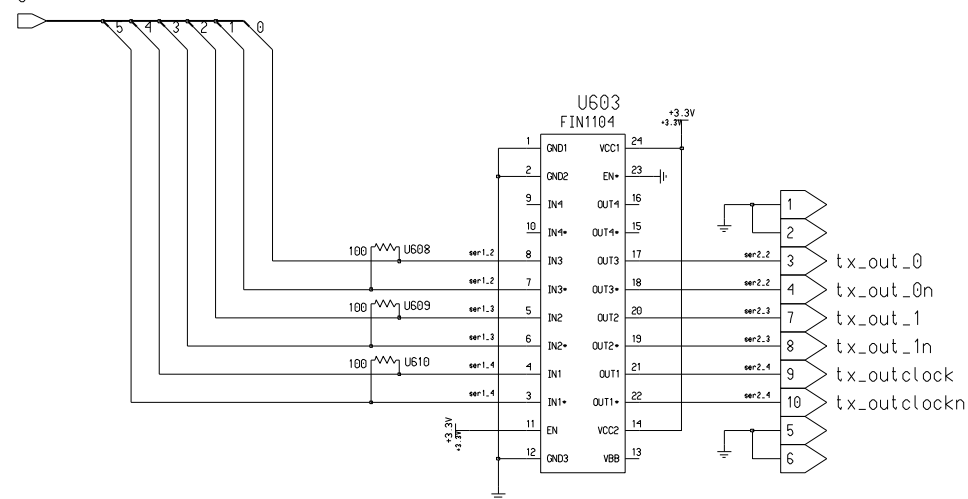


A

A

LVDS serial output  
Insert transceiver here:

DigOutSer (7:0)

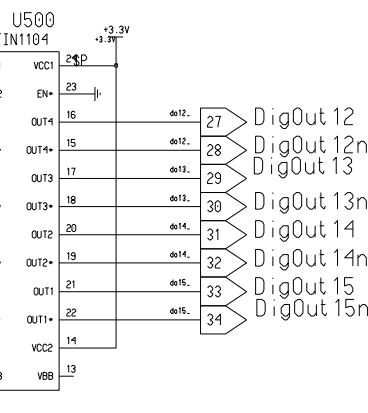
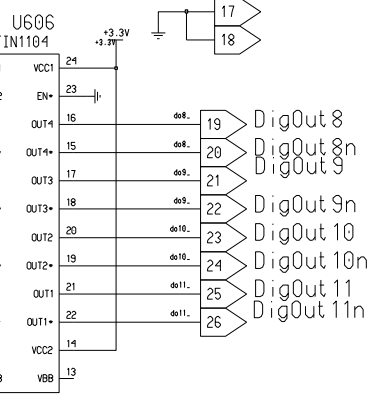
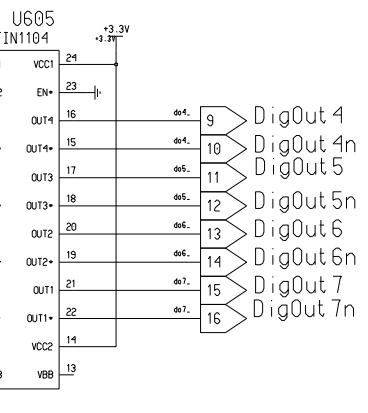


B

B

C

C



D

D

Engineer	M. Bogdan	The University of Chicago	
Drawn by	M. Bogdan	5640 S. Ellis Ave. Chicago, IL 60637	
R&D CHK		TITLE	Size C
DATE:	3/15/05	<b>Front Panel - digital output</b>	
TIME:	1:30 pm	<b>JPARC-K 14BIT-ADC Board</b>	
QA CHK		REV A	DRW. B-2605 Sheet 2 of 12