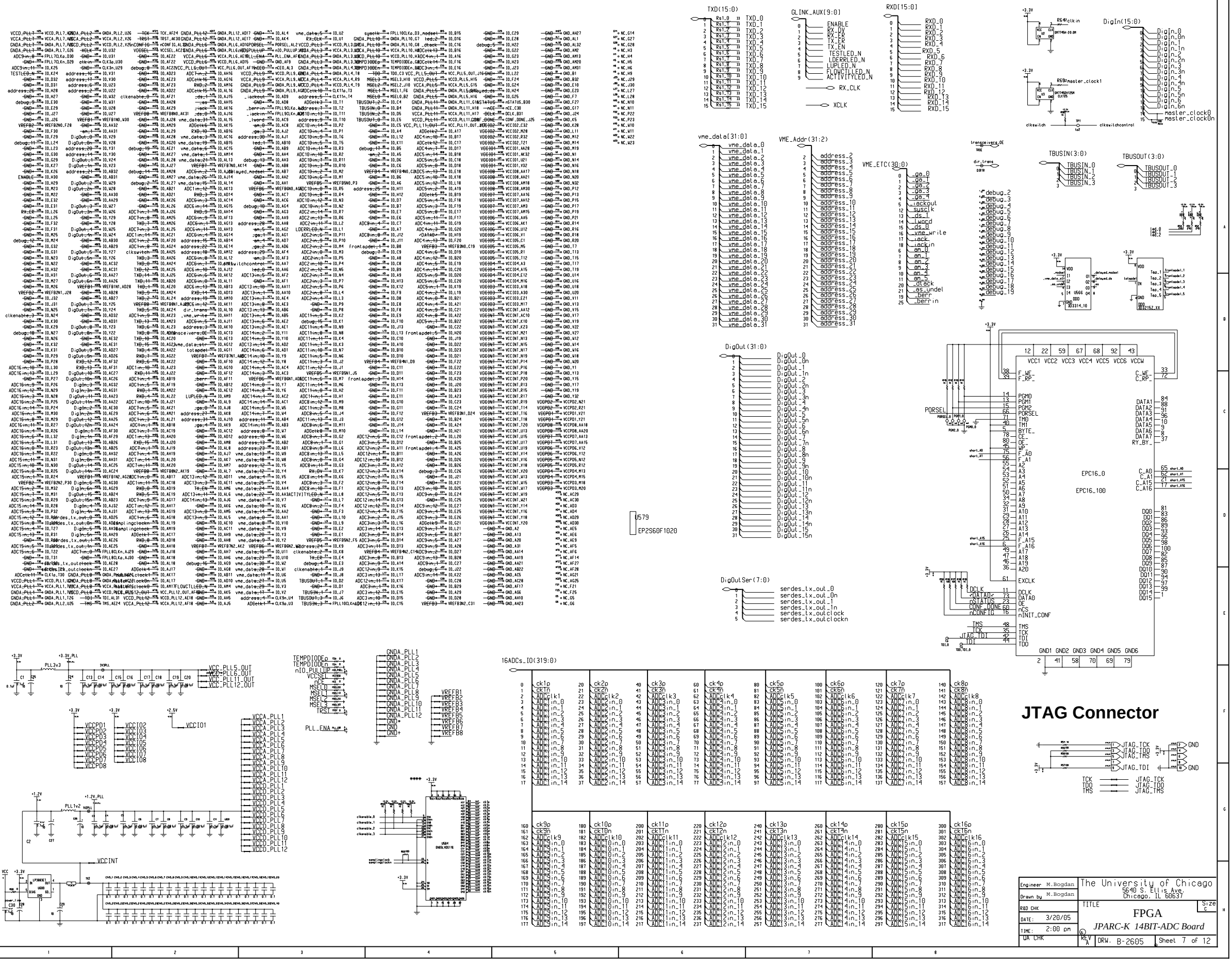
TXD(15:0)
RXD[15:0]
GLINK_AUX[9:0]
ENABLE
RX_DV
RX_ER
TX_ER
TX_EN
TESTLED_N
LDERRLED_N
LUPLED_N
FLOWCTLLED_N
ACTIVITYLED_N
RX_CLK
XCLK
DigIn(15:0)
vme_data[31:0]
VME_Addr(31:2)
VME_ETC(30:0)
DigOut(31:0)
DigOutSer(7:0)
U579
EP2S60F1020
16ADCs_IO(319:0)
JTAG Connector
JTAG_TCK
JTAG_TDO
JTAG_TMS
JTAG_TDI
EPC16_0
EPC16_100
FPGA
JPARC-K 14BIT-ADC Board
The University of Chicago
5640 S. Ellis Ave.
Chicago, IL 60637
Engineer M.Bogdan
Drawn by M.Bogdan
R&D CHK
DATE: 3/20/05
TIME: 2:00 pm
QA CHK
REV A
DRW. B-2605
Sheet 7 of 12