Board Characteristics

1. Material FR4 with Tg>170°C [e.g., FR466]
2. Minimum trace width and clearance: 0.005" on Signal 1, 1.6 (Top and Bottom)
3. Minimum trace width and clearance: 0.0025" on Signal 2, 3, 4, 5, 7, 9, 10 (all striplines)
4. 1 oz copper for all power layers and for Signal 1, 2 (Top and Bottom)
   1/2 oz copper for Stripline trace layers (Signal 3, 4, 5, 6, 7, 8, 9, 10)
5. Immersion Gold followed by copper, with min. Ni: 2.5-5 μm, Cu: 0.05-0.2 μm
   Apply Solder Wash over bare copper
6. Board Thickness: 0.032 ± 0.006
7. Fill the Top and Bottom of board on the solder side to a thickness of 0.063 ± 0.008
8. Silk-screen on Component and Solder Sides
9. 45 degree chamfer
10. Solder tolerances: ± 0.030" unless specified otherwise
11. Layer spacing as specified
12. 20 MSG Ohm ± 5 Ohm for 0.005" striplines and 0.006" microstrip traces on all layers.
    Perform TDR test for all signal layers.
    Present TDR test results for all signal layers.

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

14-BIT ADC BOARD
SPECS

DATE: 12/20/94
REV: 01

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Perform TDR test for all signal layers.
Present TDR test results for all signal layers.