FADC Boards for JPARC-K

Preliminary Proposal

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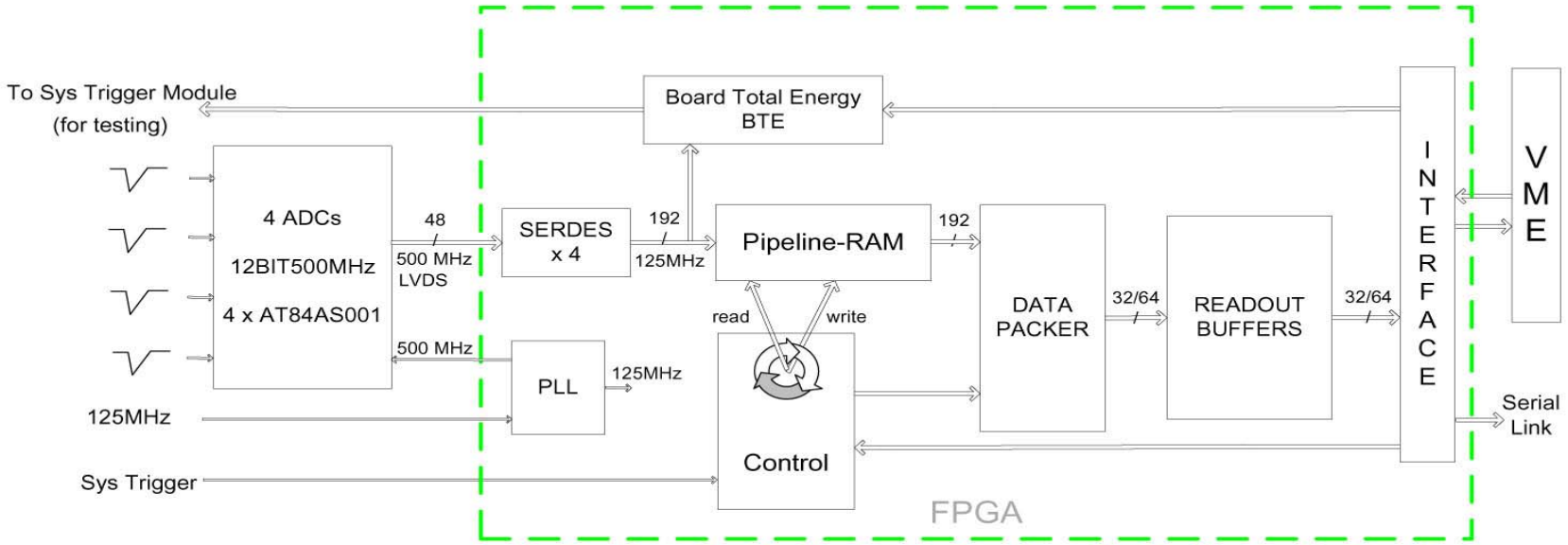
12-Bit, 500MHz FADC Board – Block Diagram

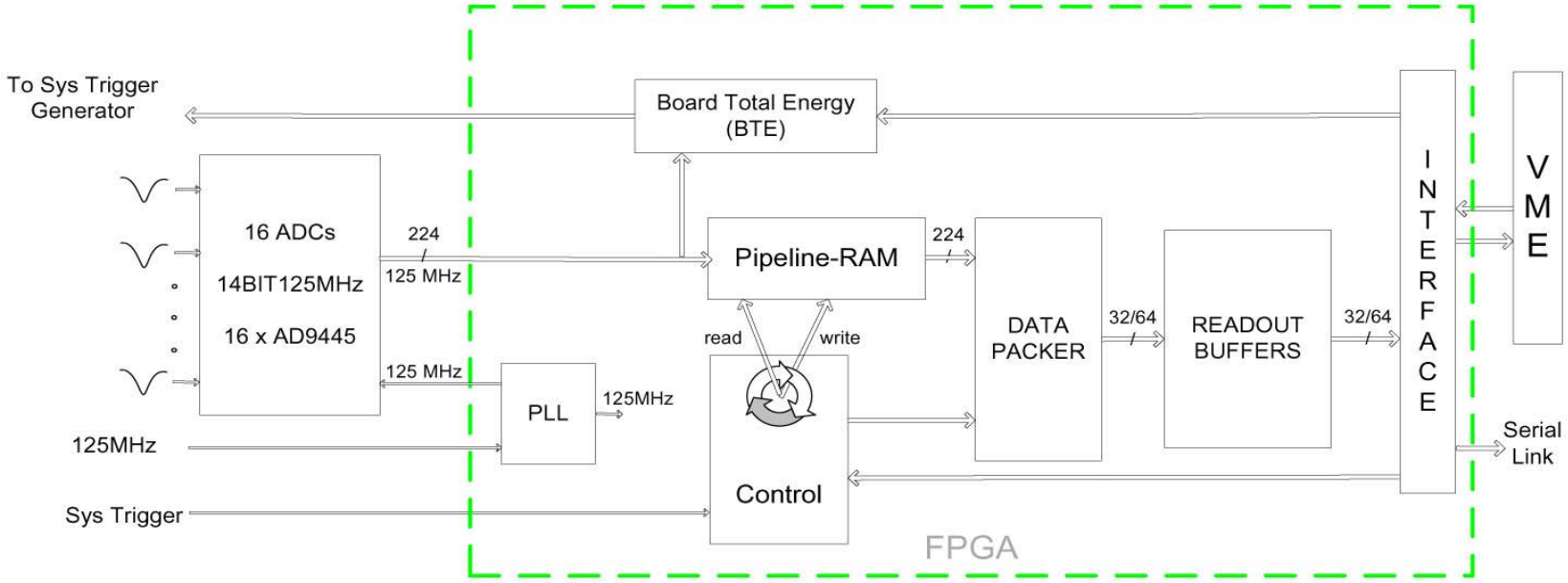


- Each FADC channel: one ATMEL - AT84AS001 chip: 12 bits/500MHz;
- One STRATIX II FPGA can service up to 4 ADC channels :
  - After SERDES, data moved with 125MHz;
  - Trigger rate: 10kHz, 64 samples/trigger (128ns);
  - Two VME readout buffers - max 128 triggers each (10 ms);
  - Input Pipeline: 25 -100us max depth (8,000 - 51,200 samples);
  - FPGA device migration possible to increase/decrease max pipeline size;

12-Bit, 500MHz FADC Board - Readout

- 4 ADC channels per Board: 6U VME32/64 with CBLT;
- Throughput with 10KHz trigger rate, 100% channel hit occupancy, 64 samples/trigger:
  - One channel: 10KHz x 12bits x 64samples = 0.96 MBPS;
  - 4-channel board: 3.84 MBPS/board;
  - Crate with 7 boards (25 channels): 24 MBPS - can be sustained via VME backplane;
  - Serial Link not needed.

14-Bit, 125MHz ADC Board – Block Diagram



- Each ADC channel - one AD9445 chip: 14 bits/125MHz;
- One STRATIX II FPGA can service 16 ADC channels:
  - Logic design similar to 500MHz FADC without SERDES;
  - Memory requirements similar to 500MHz FADC with the same time delay;
  - Trigger rate: 10kHz, 16 samples/trigger (128ns);
  - Two VME readout buffers - max 128 triggers (10 ms);
  - Input Pipeline: 25 -100us max depth (2,000 – 12,800 samples);
  - FPGA device migration possible to increase/decrease max pipeline size;

14-Bit, 125 MHz ADC Board - Readout

- 16 ADC channels per Board: 6U VME32/64 with CBLT;
- 16 ADC Boards per Crate;

- Throughput with 10 KHz trigger rate, 10% channel hit occupancy, 16 samples/trigger:
  - One channel: 10KHz x 10% x 2Bytes x 16samples = 32 KBPS;
  - 16-channel board: 512 KBPS/board
  - Crate with 16 boards: 8 MBPS - can be sustained via VME backplane;
  - Serial Link not needed.

Conclusions

- High level of reuse between the two designs; many logic blocks are the same;
- FPGA requirements are about the same for: 4-ch,500MHz and 16-ch,125MHz boards;
- Performed preliminary FPGA design tests:
  - With Altera EP2S60F1020C5 ($600): > 25us depth pipeline;
  - With Altera EP2S90F1020C5 ($1,600): > 50us depth pipeline;
  - With Altera EP2S130F1020C5 ($2,800): >100us depth pipeline;
- Memory requirements may be slightly larger on the 4-ch, 500MHz board, because of higher readout throughput per board;
- FPGA device migration possible on the same PCB.