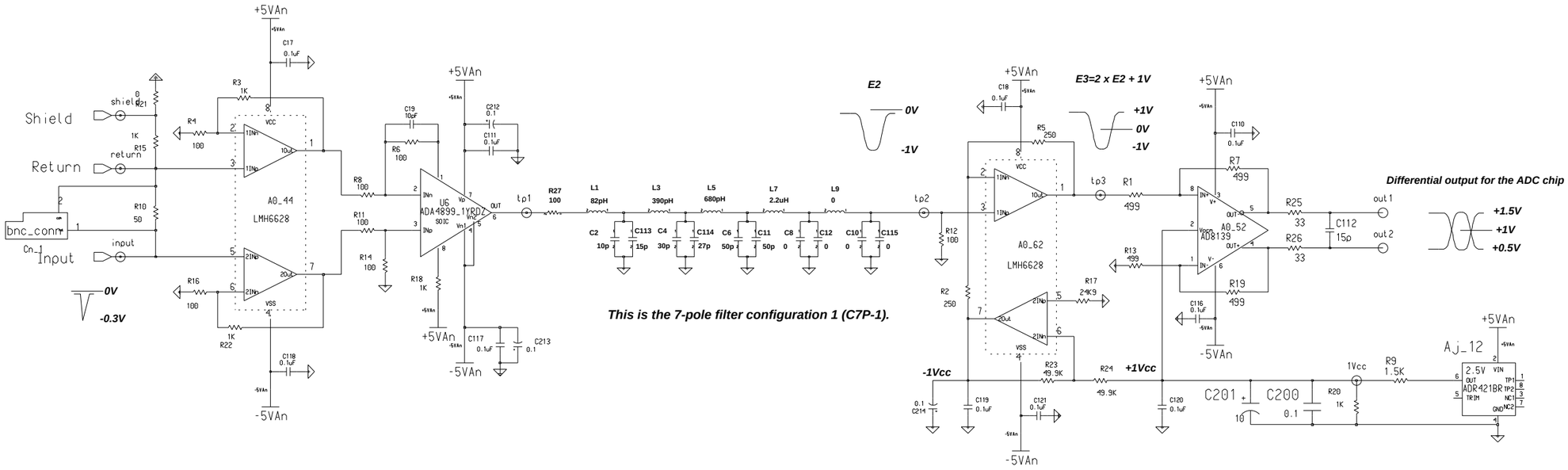

This is the 7-pole filter configuration 1 (C7P-1).

Notes:

This schematic is for testing the Preamp/Shaper/ADC_Driver circuit for the 14-Bit, 125MHz ADC Board.
The actual schematic will have the +1V level generated from the ADC chip reference output.
This circuit is designed to receive only negative pulses, the gain is adjustable by changing R3 and R22.
The values: L1,C2,L3,C4,L5,C6,L7 in the 7-pole filter determine the FWHH for the output pulse.

Testing instructions:

In this configuration the board accepts only negative input pulses between 0V and -300mV.
To test with larger input pulses, decrease the gain by changing R3 and R22.
For output testing use Tp2.
The signal amplitude on Tp2 depends on the height and width of the input pulse.
The signal amplitude on Tp2 should not exceed -1V.

Engineer	M.Bogdan	**The University of Chicago**	
Drawn by	M.Bogdan	**5640 S. Ellis Ave., Chicago, IL 60637**	
R&D CHK		TITLE	Size C
DATE:	5/30/07	Preamp/Shaper Test Board	
TIME:	11:00 am	**7-Pole Filter Configuration**	
QA CHK		REV A	DRW. B-2620 Sheet 1 of 1