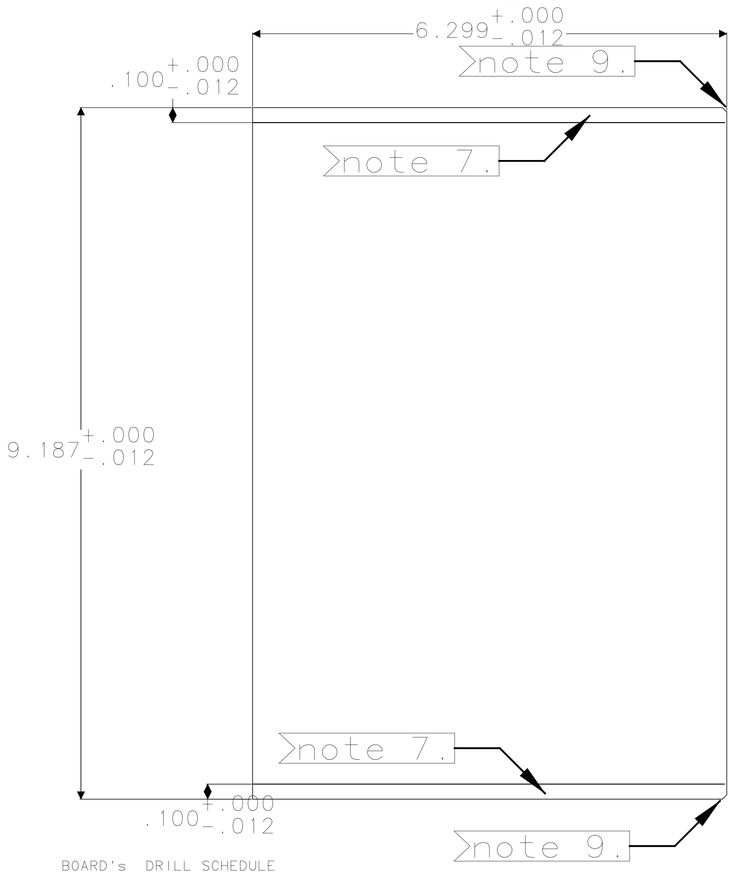
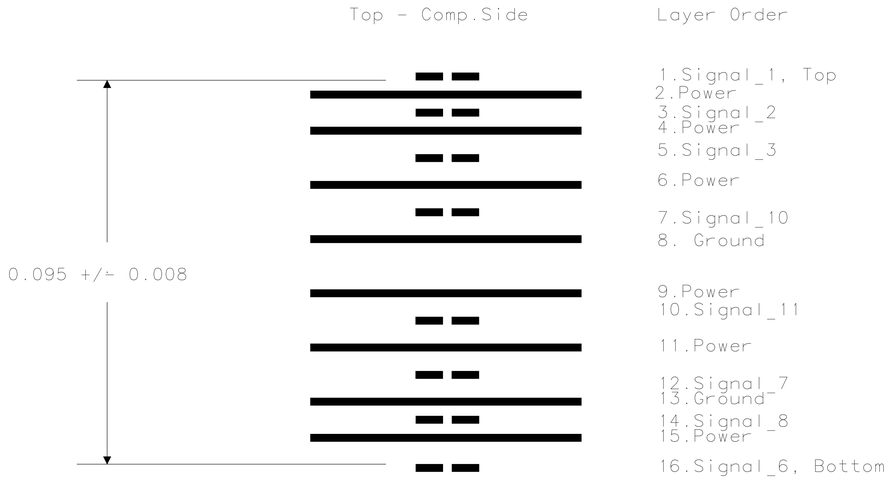
DWG.NO. 2869 | SH | REV. A



BOARD's DRILL SCHEDULE

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Tolerance	COMMENT
○	.0081	1069	YES	---	Note 13
⊞	.009	366	YES	---	
⌀	.0091	3112	YES	---	Note 13
⊟	.011811024	2	YES	---	
⊖	.0236	90	YES	---	Note 3
◫	.035	22	YES	---	
⊕	.041	617	YES	---	
□	.042	20	YES	---	
	.057	2	YES	---	
	.059	15	YES	---	
	.066	3	YES	---	
	.067	60	YES	---	
	.07	4	YES	---	
	.106	8	NO	---	
	.12598425	2	NO	---	
	.12795276	2	YES	---	
	.15	5	YES	---	
	.15	6	NO	---	



Board Characteristics - 16 LAYER BOARD

1. Material: Megtron6
2. Minimum trace width: 0.005" and clearence: 0.005";
3. This is a pressfit tech hole with the following specs:
   -Diameter of drilled hole: 0.7mm=/-0.02mm
   -Diameter of finished plated hole: 0.6mm=/-0.05mm
   -Hole Plating: min 25um Cu, 2.5-5umNi, 0.05-0.2um Au (Electroless Ni/Immersion Au)
4. 1 oz copper for all power layers and for Signal_1,2 (Top and Bottom)
   1/2 oz copper for Stripline trace layers (Signal_2,3,4,5,7,10,11,12).
5. Electroless Nickel Immersion Gold plating, with min. Ni: 2.5-5 um; Au: 0.05-0.2 um.
   Apply Solder Mask over bare copper.
6. Board Thickness: 0.093 +/- 0.008
7. Mill the Top and Bottom of board on the solder side to a remeining thickness of 0.063" +/- 0.008
8. Silkscreen on Component and Solder Sides.
9. 45 degree chamfer.
10. FHS tolerances: +/- 0.003 unless specified otherwise.
11. Interlayer spacing as specified.
12. Zc=55 Ohm, Zd=100 Ohm for all 0.005" traces.
    Perform TDR test for all signal layers.
    Present TDR test results for all signal layers.
13. Via Fill and Overplate:
    Vias of this diameter must be completely filled with Peters PP-2795 or equivalent,
    planarized, and plated over with Copper and surface finish.
    The plated cap must adhere to fill material after 1x 550F solder shock.
14. Remove all non-functional inner layer pads for pins and vias.
15. Do not increas size of thermal pads and associated spoke connections on 0.041" and 0.0413" holes.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX
.XXX
DO NOT SCALE DRAWING

TREATMENT

FINISH

SIMILAR TO | ACT. WT | CALC WT

CONTRACT NO.

APPROVALS		DATE
DRAWN	M.Bogdan	6/22/2016
CHECKED	M.Bogdan	6/22/2016
ISSUED		

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE: 1,500MSPS ADC Module Specification Drawing

SIZE B | FSCM NO. | DWG. NO. 2869 | REV. A

SCALE 1/2 | SHEET

THIS SHEET IS COMPUTER GENERATED