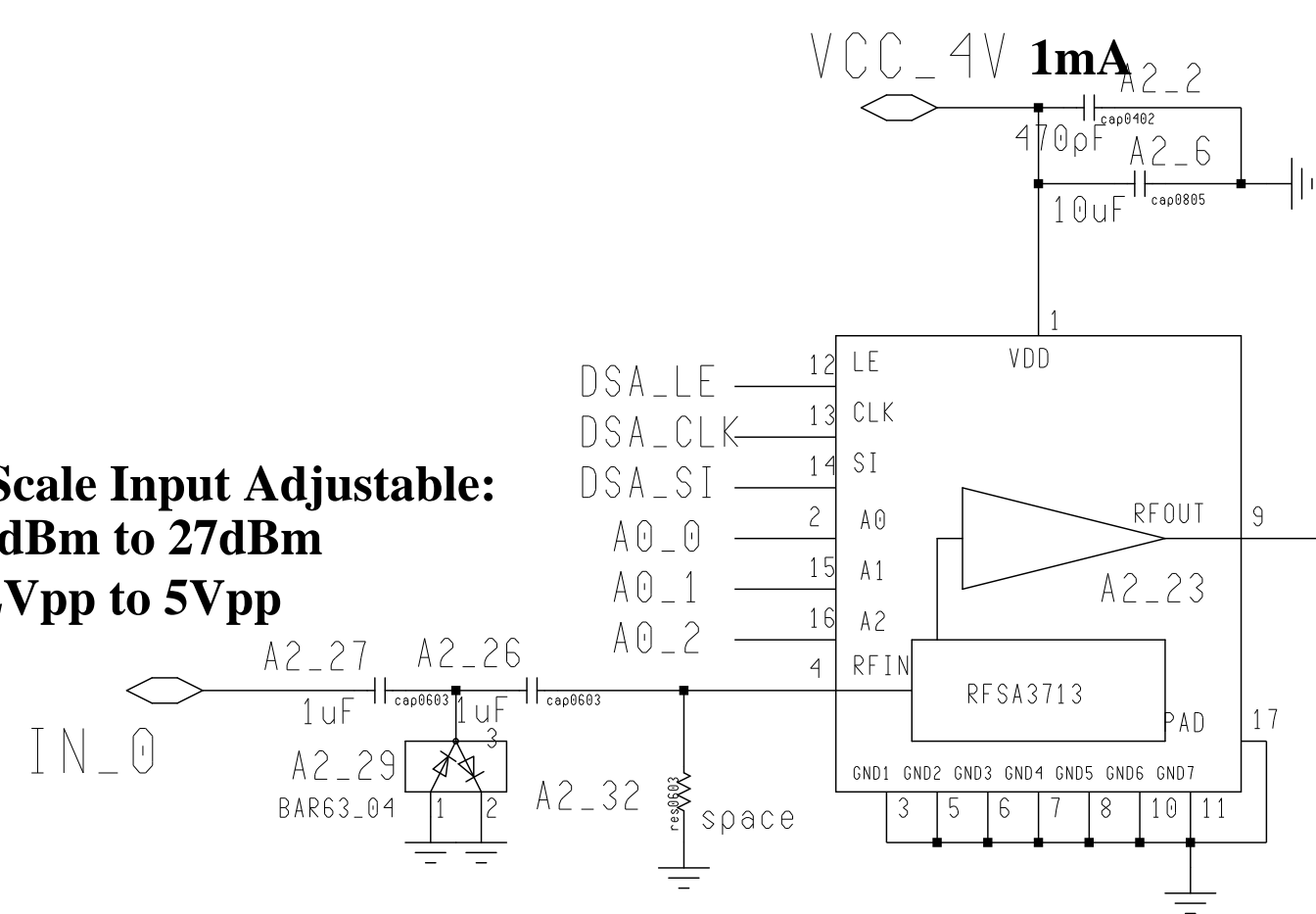


Max 3dB Bandwidth: 2,400MHz

Digital Step Attenuator - 31dB gain control range

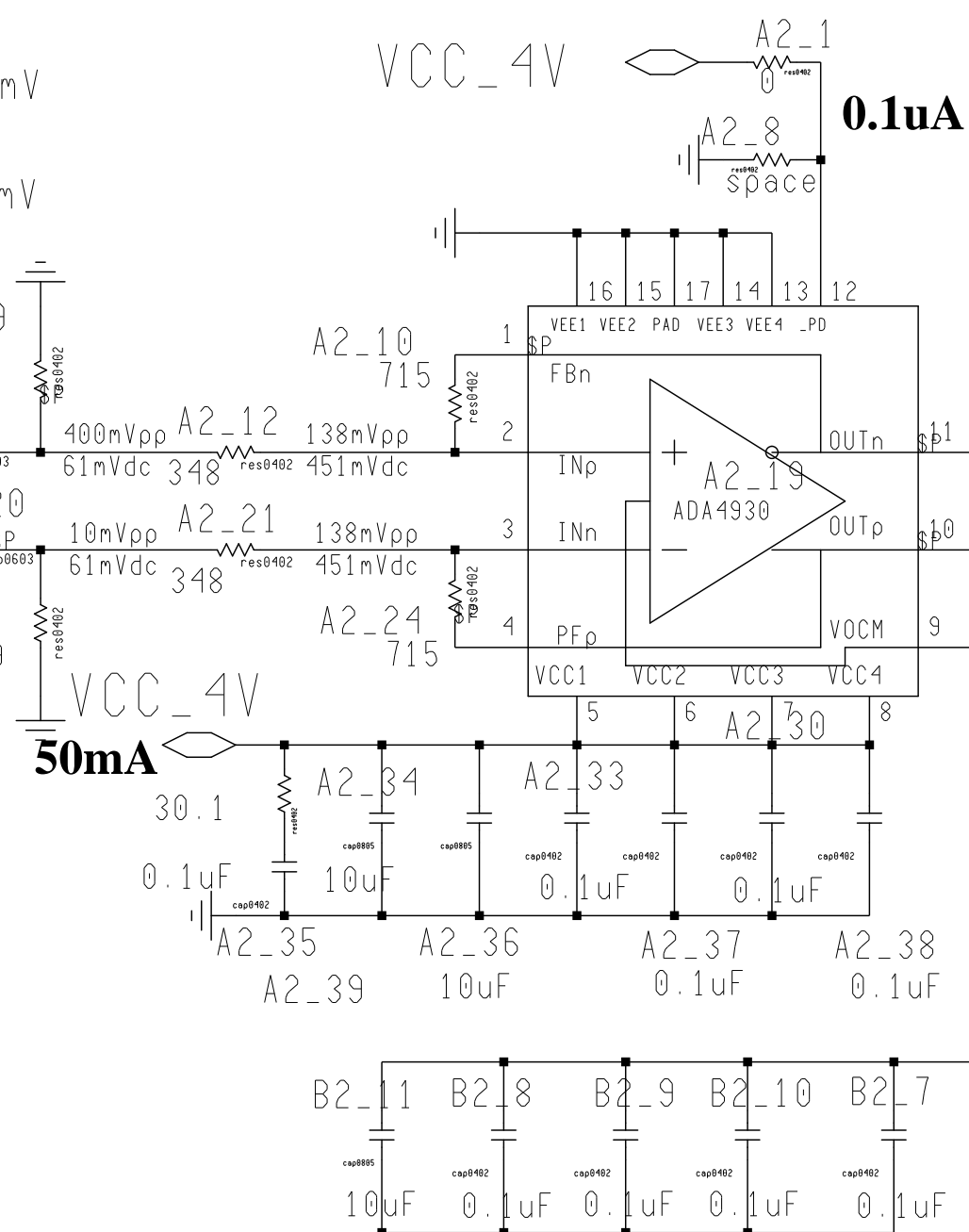
Full Scale Input Adjustable:
-1.6dBm to 27dBm
0.2Vpp to 5Vpp



Actual Gain: 5 - Fixed

Max -3dB Bandwidth: 807MHz

Actual Gain: 1 - Fixed

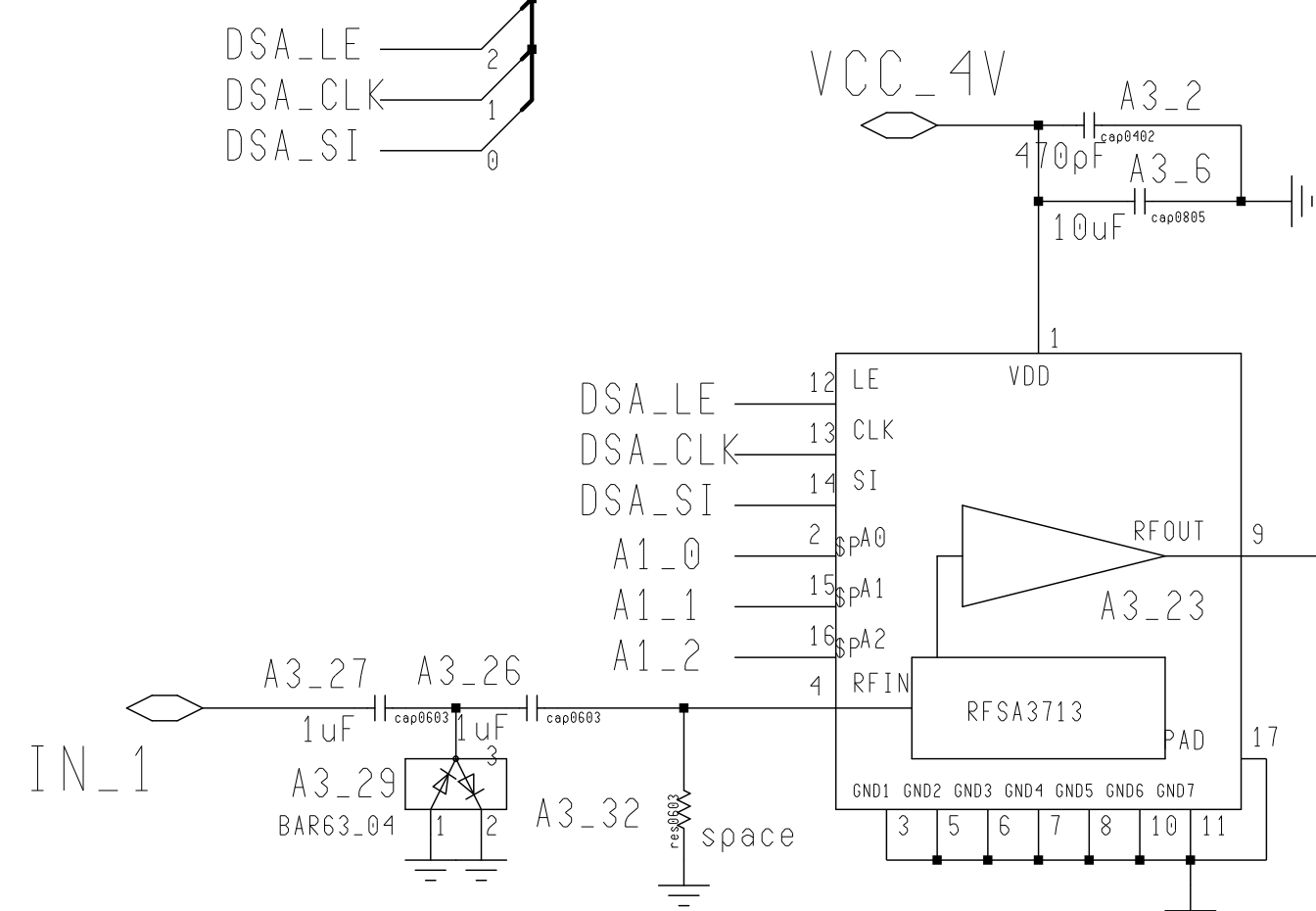


Digital Step Attenuator Control

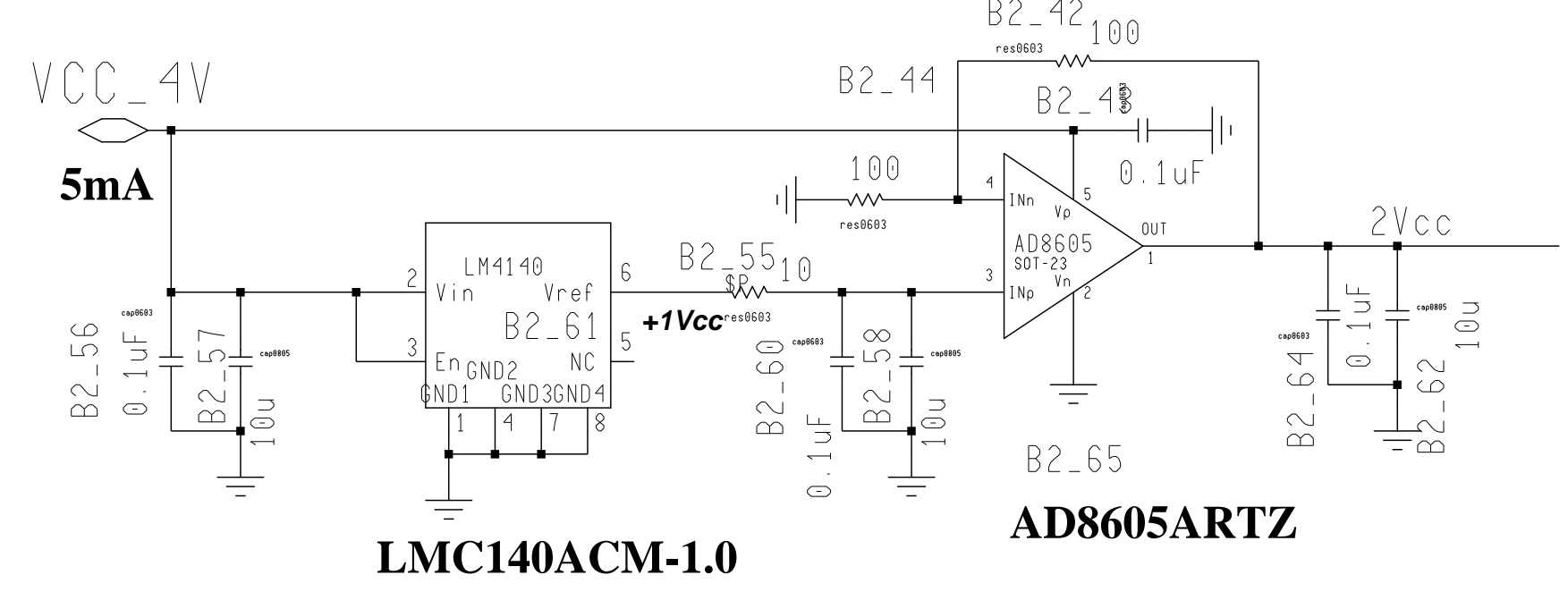
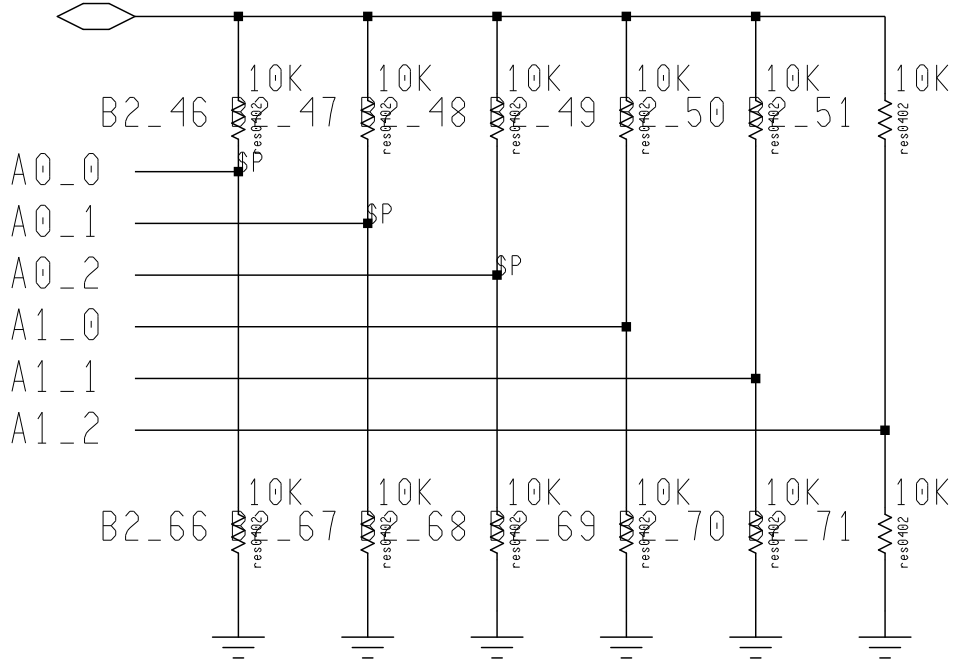
From FPGA - 2.5V I/O Bank

Lines are bussed for all 8 attenuators

DSA_CTRL[2:0]



Address Hardwired



ADC_CTRL[3:0]

From FPGA - 1.8V I/O Bank

ADC_CTRL_COM[3:0]

Shared Lines

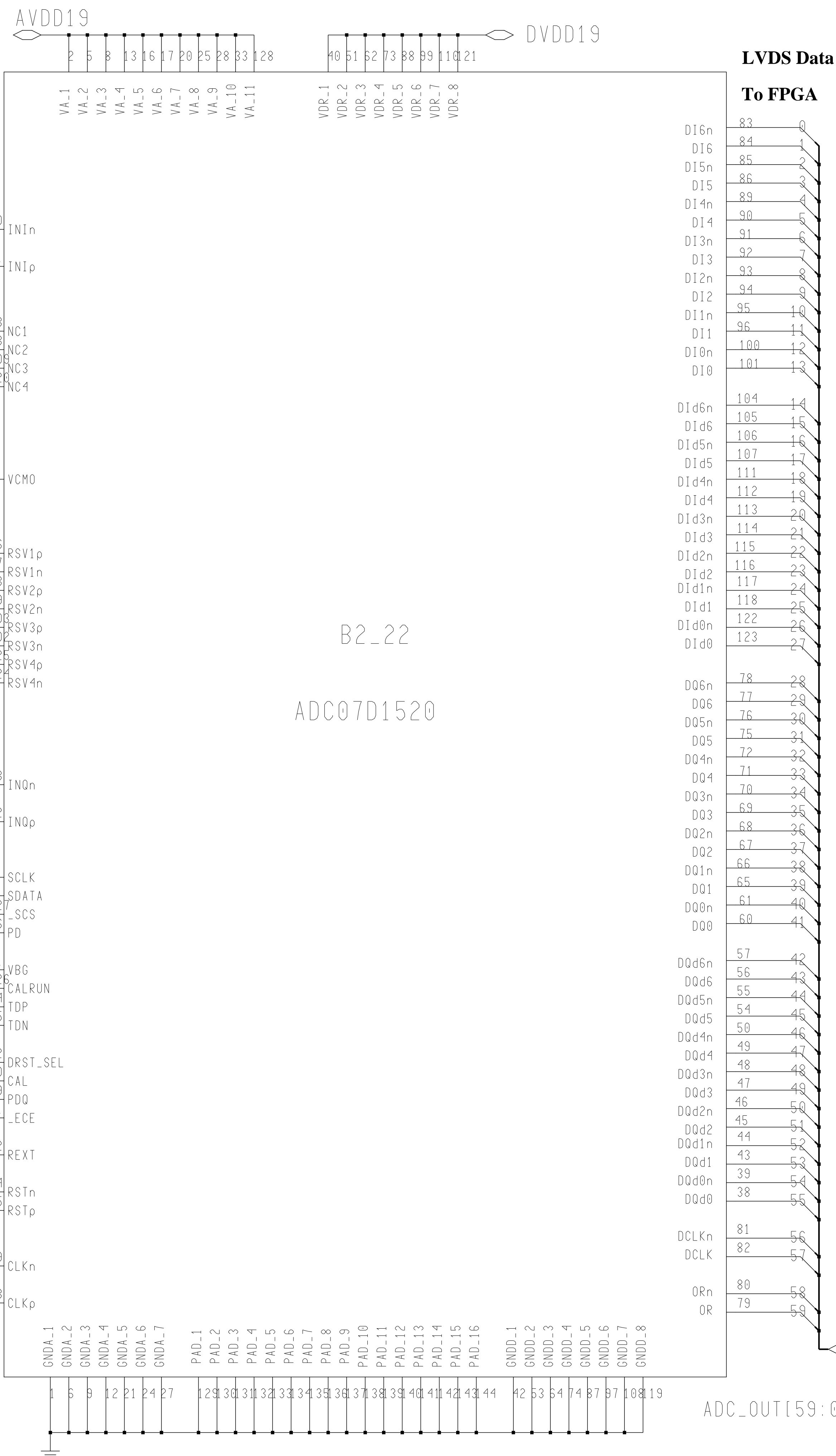
From FPGA - 1.8V I/O Bank

ADC_SYNC[1:0]

From FPGA

ADC_CLK[1:0]

From PLL



Notes:
If resistors A0_18, A1_18 are installed, the Fixed Gain Amplifiers A0_17, A1_17 shall not be installed.
In this case, the overall gain is reduced by a factor of 5.

POWER:
4Vcc - 200mA max
1.9V for AVDD19 - 1A max
1.9V for DVDD19 - 0.3A max

Engineer: M. Bogdan	The University of Chicago ADC Channel 2 and 3 1500MHz ADC Module	
Drawn by: M. Bogdan		
DATE: 5/5/2016		
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