Max 3dB Bandwidth: 2,400MHz

Digital Step Attenuator - 31dB gain control range

Actual Gain: 5 - Fixed

Max -3dB Bandwidth: 807MHz

Actual Gain: 1 - Fixed

Full Scale Input Adjustable:
-1.6dBm to 27dBm
0.2Vpp to 5Vpp

-3dBm

1mA

50mA

0.1uA

50mA

1mA

AD8605ARTZ

LVDS Data

To FPGA

Digital Step Attenuator Control

From FPGA - 2.5V I/O Bank

Lines are bussed for all 8 attenuators

Address Hardwired

5mA

LMC140ACM-1.0

AD8605ARTZ

From FPGA - 1.8V I/O Bank

Shared Lines
From FPGA - 1.8V I/O Bank

From FPGA

From PLL

Notes:
If resistors A0_18, A1_18 are installed, the Fixed Gain Amplifiers A0_17, A1_17 shall not be installed.
In this case, the overall gain is reduced by a factor of 5.

POWER:
4Vcc - 200mA max
1.9V for AVDD19 - 1A max
1.9V for DVDD19 - 0.3A max

Engineer: M. Bogdan	**The University of Chicago**
Drawn by: M. Bogdan	ADC Channel 6 and 7
DATE: 5/5/2016	*1500MHz ADC Module*
REV. A	DRW. 2868
	Sheet 12-4