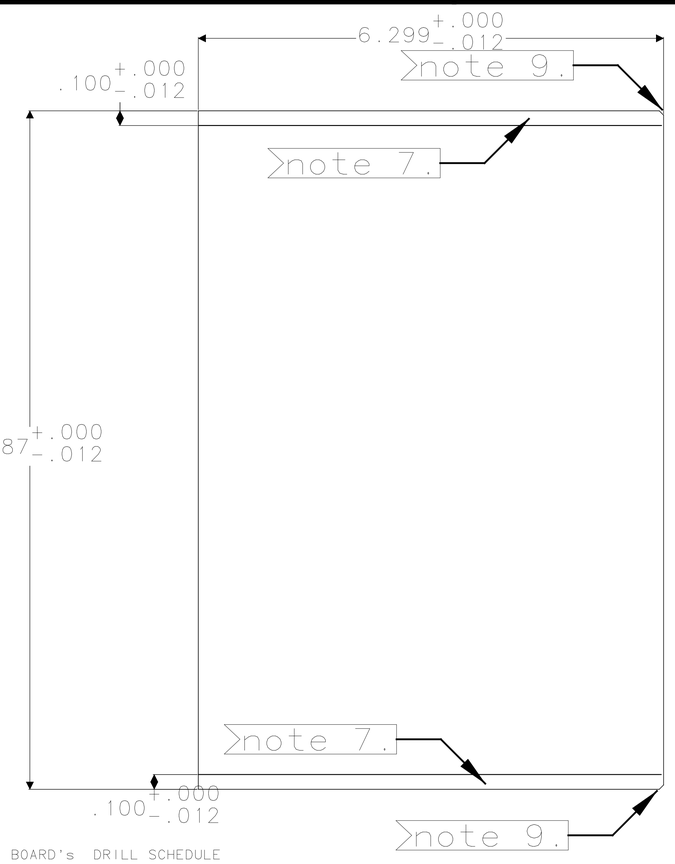
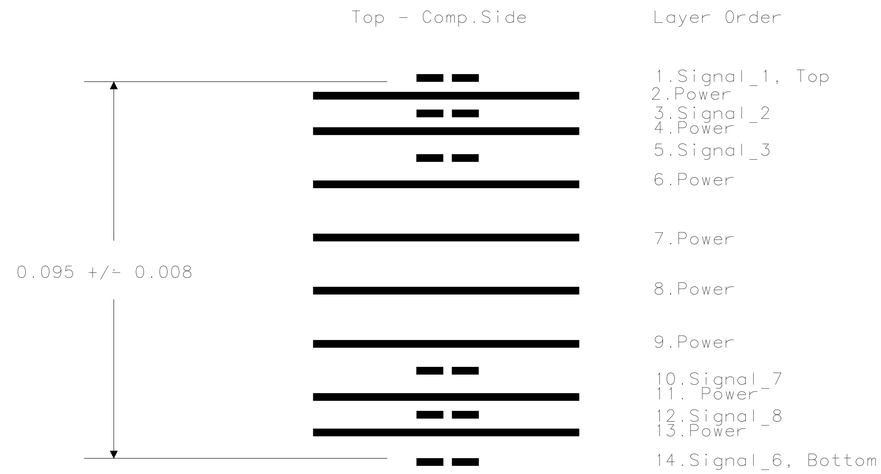
DWG.NO. 2866 | SH | REV. A



BOARD's DRILL SCHEDULE

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Tolerance	COMMENT
○	.009	1532	YES	---	
⊞	.0091	2538	YES	---	Note 13
⌀	.011811024	10	YES	---	
⊟	.02	4	YES	---	
⊖	.033464567	2	YES	---	
◫	.035	14	YES	---	
⊕	.037401575	18	YES	---	
□	.041	530	YES	---	
	.041338583	20	YES	---	
	.042	20	YES	---	
	.052	10	YES	---	
	.057	6	YES	---	
	.061023622	4	YES	---	
	.062	8	YES	---	
	.06496063	2	NO	---	
	.066	2	YES	---	
	.07	4	YES	---	
	.106	4	NO	---	
	.10629921	2	YES	---	
	.12598425	2	NO	---	
	.12795276	2	YES	---	
	.15	8	NO	---	



Board Characteristics - 14 LAYER BOARD

1. Material: Megtron6
2. Minimum trace width: 0.006" and clearence: 0.005" on Signal_1,6 (Top and Bottom);
3. Minimum trace width and clearence: 0.005" on Signal_2,3,4,5,7,8,9,10,11,12 (all stripline);
4. 1 oz copper for all power layers and for Signal_1,2 (Top and Bottom)
   1/2 oz copper for Stripline trace layers (Signal_2,3,4,5,7,10,11,12).
5. Electroless Nickel Immersion Gold plating, with min. Ni: 2.5-5 um; Au: 0.05-0.2 um.
   Apply Solder Mask over bare copper.
6. Board Thickness: 0.093 +/- 0.008
7. Mill the Top and Bottom of board on the solder side to a remaining thickness of 0.063" +/- 0.008
8. Silkscreen on Component and Solder Sides.
9. 45 degree chamfer.
10. FHS tolerances: +/- 0.003 unless specified otherwise.
11. Interlayer spacing as specified.
12. Zc=55 Ohm, Zd=100 Ohm for all 0.005" stripline and all 0.006" microstrip traces.
    Perform TDR test for all signal layers.
    Present TDR test results for all signal layers.
13. Via Fill and Overplate:
    Vias of this diameter must be completely filled with Peters PP-2795 or equivalent,
    planarized, and plated over with Copper and surface finish.
    The plated cap must adhere to fill material after 1x 550F solder shock.
14. Remove all non-functional inner layer pads for pins and vias.
15. Do not increas size of thermal pads and associated spoke connections on holes.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX
.XXX
DO NOT SCALE DRAWING

TREATMENT

FINISH

SIMILAR TO | ACT.WT | CALC WT

CONTRACT NO.

APPROVALS	DATE
DRAWN M.Bogdan	4/25/2016
CHECKED M.Bogdan	4/25/2016
ISSUED	

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
20-BIT ADC Board
Specification Drawing

SIZE B | FSCM NO. | DWG.NO. 2866 | REV. A

SCALE 1/2 | SHEET

THIS SHEET IS COMPUTER GENERATED