Custom 16-Channel, 12-Bit, 500MHZ ADC Module for the KOTO Experiment at J-PARC

Mircea Bogdan, Yau Wah
The University of Chicago

This paper presents a custom 16-Channel, 12-Bit, 500 MHz ADC/Data Processing Module, designed for the KOTO Experiment at the Japan Proton Accelerator Research Complex (J-PARC). Few hundreds of this 6U VME board will receive signals from various detectors of the apparatus, and will be the digitizing modules in the Experiment's Data Acquisition System (DAQ). In KOTO, the main ADC/DAQ system runs at a 125 MHz simultaneous sampling rate, provided by one low jitter 125 MHz system clock. The 500 MHz ADC Module receives this system clock and multiplies its frequency by four with an internal PLL. The 16 analog input pulses are passed to 8 dual channel ADC chips (ADS5407). After sampling, data are processed locally with two Field Programmable Gate Arrays (FPGA). The module is equipped with a pipeline up to 40us (20,480 samples) long, where digitized values are stored, awaiting the system Level 1 trigger. After the trigger, data are packed and buffered for readout. The readout can be performed via the VME32/64 backplane, or via the two front panel QSFPs at rates of up to 48Gbps. Designed specifically for the KOTO Experiment, this module can also be used in many other Physics applications. The design and preliminary test results will be described.

Introduction

The KOTO experiment is dedicated to observe $K_L \to \pi^0 \nu\nu$ decay using the 30-GeV proton beam at the Japan Proton Accelerator Research Complex (J-PARC) [1]. The $K_L \to \pi^0 \nu\nu$ is a direct CP-violating and flavor-changing neutral current process. The branching ratio (BR) is proportional to the square of the CP violation parameter η in the CKM matrix [2] and is predicted to be 2.43×10^{-11} in the Standard Model (SM) [3]. The attractive features of the decay include the exceptionally small theoretical uncertainty of the BR of on 2-3%. Therefore measurement of the BR of this decay mode is highly sensitive to the contribution of new physics beyond the SM. The experimental upper limit on the BR was set to be 2.6×10^{-8} at 90% confidence level by the E391a experiment at KEK [4]. The KOTO experiment [5,6] aims to reach a sensitivity below 10^{-11} by utilizing the high intensity beam at J-PARC. To collect data with the vastly increased beam intensity, a pipeline DAQ system has been designed.

We present here a custom ADC/DAQ module designed for such purpose for the DAQ system.

Architecture

The Block Diagram for one half of the ADC module is presented in Figure 1. We can identify three main blocks: the signal conditioning and conversion block, the data processing block, and the interface block.

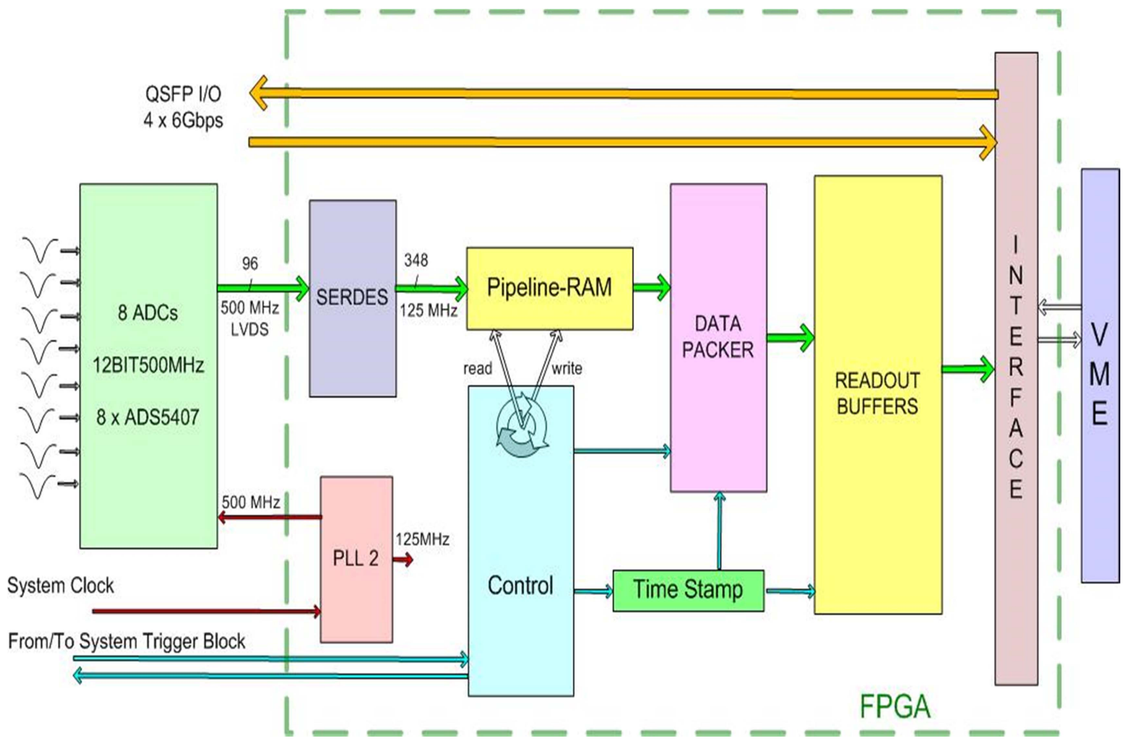

Figure1. Block Diagram for half of the 500MHz ADC Module. Eight channels are serviced by one single Altera ARRIA V FPGA [7]. The 500 MHz digitized samples are first deserialized and reduced in frequency by a factor of four. All subsequent data processing steps take place at the 125MHz system clock frequency.

Figure 2 presents the Schematic of one analog channel, configured to run with an offset differential input signal as provided in the KOTO experiment. The input channel bandwidth is about 125MHz at -3dB. The analog signal is amplified, offset, and applied to the A/D chip ADS5407, by TI.

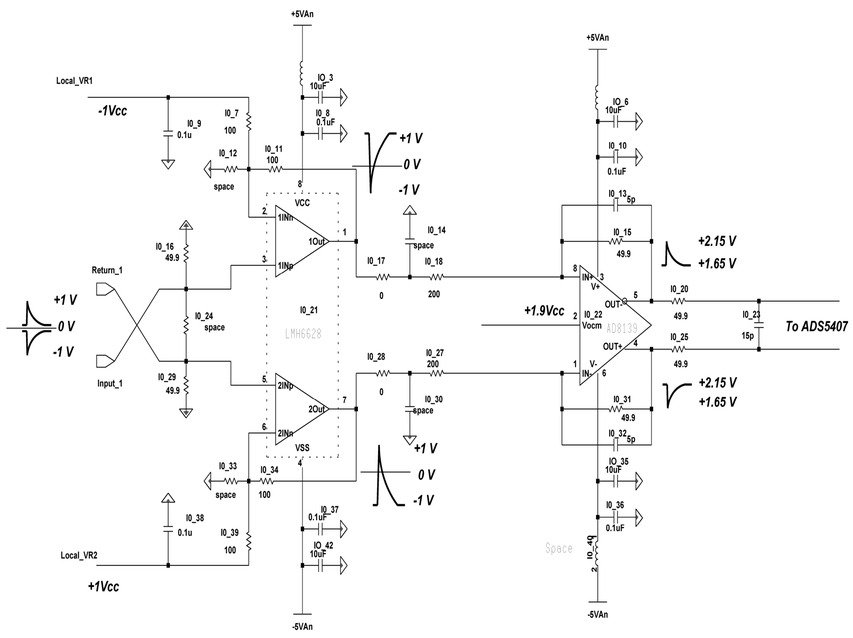

Figure 2. Schematic of one ADC input channel.

Signal gain, offset, and bandwidth can be adjusted by changing a few passive components. Any channel can be independently configured for a differential or for a single-ended input signal.

In the KOTO Experiment, this module will work on the 125MHz system clock, applied to a PLL inside of each one of the FPGAs, which provides the 500MHz sampling clocks.

The module is provided with two QSFP transceivers with up to 6Gbps per link, for a total of 48Gbps. Depending on the application and data rate requirements, all 16 channels can be read out from any of the QSFPs, or from both.

Conclusions

Figure 3 presents one of the ADC modules. Preliminary test results show an input noise of about 1.3 LSB for a sampling rate of 500MHz, and with a one-pole input filter at about 125MHz.

This small and powerful ADC module was designed to be used in the KOTO DAQ System, but it can also offer a great level of configurability. With minor firmware changes, and/or passive component modifications, this module can easily be integrated for many other applications.

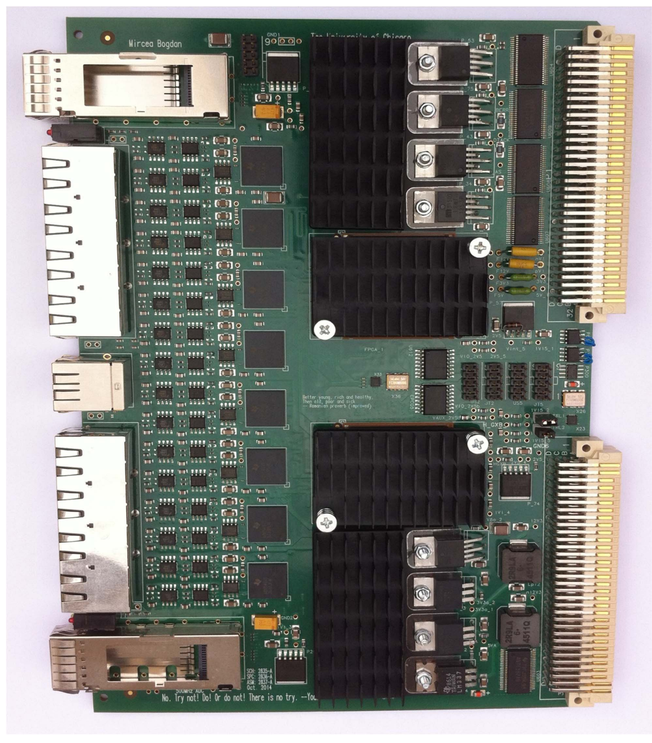

Figure 3. Prototype 16-Channel 500MSPS ADC/DAQ Module. This PCB was designed for analog inputs received on RJ45 connectors.

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