# Custom 16-Channel, 12-Bit, 500MHZ ADC Module for the KOTO Experiment at J-PARC

Mircea Bogdan, Yau Wah

***Abstract*–This paper presents a 16-Channel, 12-Bit, 500 MHz ADC/Data Processing Module, designed for the KOTO Experiment at the Japan Proton Accelerator Research Complex (J-PARC). Few hundreds of this 6U VME board will receive signals from various detectors of the apparatus, and will be the digitizing modules in the Experiment's Data Acquisition System (DAQ). In KOTO, the main ADC/DAQ system runs at a 125 MHz simultaneous sampling rate, provided by one low jitter system clock. The 500 MHz ADC Module receives this system clock and multiplies its frequency by four with an internal PLL. The 16 analog input pulses are passed to 8 dual channel ADC chips (ADS5407). After sampling, data are processed locally with two Field Programmable Gate Arrays (FPGA). The module is equipped with a pipeline up to 40us (20,480 samples) long, where digitized values are stored, awaiting the system Level 1 trigger. After the trigger, data are packed and buffered for readout. The readout can be performed via the VME32/64 backplane, or via the two front panel QSFPs at rates of up to 48Gbps. Designed specifically for the KOTO Experiment, this module can also be used in many other Physics applications. The design and preliminary test results will be described.**

## I. Introduction

THE KOTO experiment is dedicated to observe $K_L \rightarrow \pi^0 \nu\nu$ decay using the 30-GeV proton beam at the Japan Proton Accelerator Research Complex (J-PARC) [1]. The $K_L \rightarrow \pi^0 \nu\nu$ is a direct CP-violating and flavor-changing neutral current process. The branching ratio (BR) is proportional to the square of the CP violation parameter $\eta$ in the CKM matrix [2] and is predicted to be $2.43 \times 10^{-11}$ in the Standard Model (SM) [3]. The attractive features of the decay include the exceptionally small theoretical uncertainty of the BR of on 2-3%. Therefore measurement of the BR of this decay mode is highly sensitive to the contribution of new physics beyond the SM. The experimental upper limit on the BR was set to be $2.6 \times 10^{-8}$ at 90% confidence level by the E391a experiment at KEK [4]. The KOTO experiment [5,6] aims to reach a sensitivity below $10^{-11}$ by utilizing the high intensity beam at J-PARC. To collect data with the vastly increased beam intensity, a pipeline DAQ system has been designed.

We present here a custom ADC/DAQ module designed for such purpose for the DAQ.

Manuscript received November 10, 2015.

Mircea Bogdan is with The University of Chicago, Chicago, IL 60637, USA (telephone: 773-834-8483, e-mail: mbogdan@uchicago.edu).

Yau Wah is with The University of Chicago, Chicago, IL 60637, USA (telephone: 773-702-7592, e-mail: ywah@uchicago.edu).

## II. Architecture

The Block Diagram for one half of the ADC module is presented in Figure 1. We can identify three main blocks: the signal conditioning and conversion block, the data processing block, and the interface block.

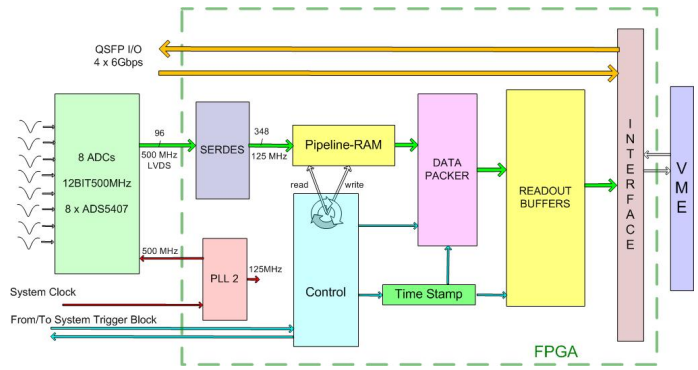


Fig. 1. Block Diagram for half of the 500MHz ADC Module. Eight channels are serviced by one single Altera ARRIA V FPGA. The 500 MHz digitized samples are first deserialized and reduced in frequency by a factor of four. All subsequent data processing steps take place at the 125MHz system clock frequency.

### A. Signal Conditioning and Conversion Block

Figure 2 presents the Schematic of one analog channel, configured to run with an offset differential input signal as provided in the KOTO experiment. The input channel bandwidth is about 130MHz at -3dB. The analog signal is amplified, offset and applied to the A/D chips ADS5407.

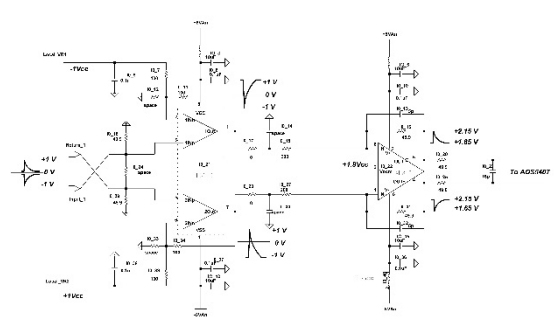

Fig. 2. Schematic of one ADC input channel.

Signal gain, offset, and bandwidth can be adjusted by changing a few passive components. Any channel can be independently configured for a differential or for a single-

ended input signal. In the KOTO Experiment, this module will work on the 125MHz system clock, applied to a PLL inside of each one of the FPGAs, which provides the 500MHz sampling clocks.

### B. Data Processing Block

Four dual ADC chips ADS5407 are serviced by one single FPGA, Altera 5AGXFB3H4F35C chip from the ARRIA V Family [7]. Each ADC chip has a simple Serial Peripheral Interface (SPI), accessible via VME and used for initial register configuration, or for test pattern generation. Depending on the application, various run modes, decimation filters, data formats, or auto correction algorithms can be enabled. Through SPI, the ADS5407 devices can also be configured into a stand-by, light or deep sleep power mode. This feature can be useful, considering that, in full run mode the total power consumption for the module is around 50W.

The ADS5407 has two ADCs and each of them consists of two interleaved converters, operating at half the sampling rate and at 180 degrees out of phase from each other. For this reason, there is a gain/timing mismatch between the resulting two interleaving products, the "odd" and the "even" recorded values. To address this mismatch, the chip is provided with auto correction circuitry which can be enabled via SPI. However, enabling the internal auto correction circuitry increases the power consumption, and also eliminated the DC component from the recorded analog signal. If the DC component is needed, the mismatch correction between the "odd" and "even" samples has to be done with a calibration block inside the FPGA, or offline, after data has been recorded and stored. On the prototypes tested, this interleaving mismatch was measured to add between 1 and 2 LSBs to the module's actual equivalent input noise.

The 500 MHz digitized samples are passed directly to the FPGAs, were data streams are first deserialized and reduced in frequency by a factor of four. All subsequent data processing steps take place at the 125MHz system clock frequency. A configurable 20,024-word Dual Access RAM, internal to each FPGA, is used to pipeline the data streams until a trigger pulse is received. After a trigger, data are packed and buffered for readout. Depending on the volume, readout can be performed via the two front panel QSFPs, or via the VME backplane. Up to 40us of latency can be implemented. This module can also run in a self-trigger mode, based on adjustable threshold levels.

For all the 16 ADC channels on the board, there are two identical FPGAs with very similar functionalities. The top FPGA is the Master and it includes the VME interface block. Communication between the two devices can be done via four 16-bit bidirectional buses.

### C. Interface Block

System interfacing is done using four LVDS signals through an RJ45 connector placed on the front panel. There are three inputs to the board, the system clock and two trigger lines, going to both FPGAs at the same time. The one LVDS output is driven only by the Master FPGA.

The module is provided with two QSFP transceivers with up to 6Gbps per each link, for a total data rate of 48Gbps. The links lead to the two internal FPGAs and their functionalities are configurable to serve different purposes. Depending on the application and date rate requirements, all 16 channels can be read out from any of the QSFPs, or from both.

## III. Conclusions

Figure 3 presents one of the ADC prototypes implemented in Chicago. Preliminary test results show an input noise of about 1.3 LSB for a sampling rate of 500MHz, and with a one-pole input filter at about 125MHz.

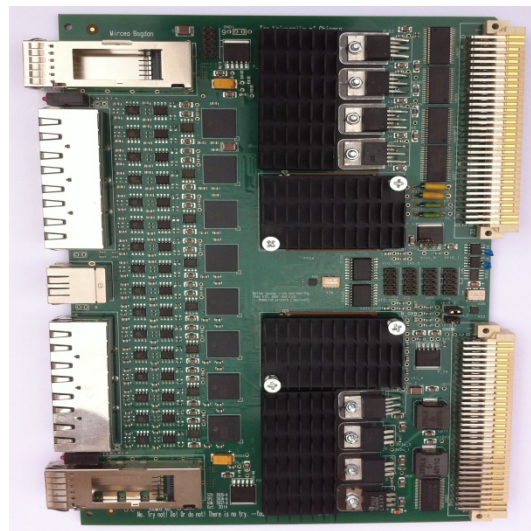

Fig. 3. Prototype 16-Channel 500MSPS ADC/DAQ Module. This PCB was designed for analog inputs received on RJ45 connectors.

This small and powerful ADC module was designed to be used in the KOTO DAQ System, but it can also offer a great level of configurability. With minor firmware changes, and/or passive component modifications, this module can easily be integrated for many other applications.

.

## References


[1] J-PARC (http://j-parc.jp/)

[2] L. Wolfenstein, Phys. Rev Lett. (1983) 1945.

[3] J. Brod, M. Gorbahn, and E. Stamou, Phys. Rev. D83 (2011) 034030.

[4] J. K. Ahn et al., Phys Rev D81 (2010) 072004.

[5] J. Comfort et al. (J-PARC E14 Collaboration),' Proposal for $K_L \rightarrow \pi^0 \nu\nu$ Experiment at J-PARC' (2006) ; Spokesman : Y. Wah ( University of Chicago, and T. Yamanaka (Osaka University). (Available at : http://j-parc.jp/researcher/Hadron/ en/ pac_0606/pdf/p14-Yamanaka.pdf).

[6] M. Togawa, Proceeding of 2013 Kaon Physics International Conference (KAON13), University of Michigan, Michigan, USA, April 29-30 and May 1st, 2013 (pos(KAON13)034).

[7] Altera Corporation, ARRIA V Device Handbook, AV-5V2, 2015.01.23