



Notes:  
The components marked "space" shall not be installed.

Engineer: <b>M. Bogdan</b>	<b>The University of Chicago</b> ADC Channel 10 and 11 500MHz 16 Ch ADC Module	
Drawn by: <b>M. Bogdan</b>		
DATE: <b>10/9/2014</b>		
REV. A	DRW. <b>2835</b>	Sheet <b>4_5</b>

DA0	H4	0
DA0n	H3	1
DA1	J2	2
DA1n	J1	3
DA2	J4	4
DA2n	J3	5
DA3	K2	6
DA3n	K1	7
DA4	K4	8
DA4n	K3	9
DA5	L2	10
DA5n	L1	11
DA6	L4	12
DA6n	L3	13
DA7	M2	14
DA7n	M1	15
DA8	M4	16
DA8n	M3	17
DA9	P1	18
DA9n	N1	19
DA10	P2	20
DA10n	N2	21
DA11	P3	22
DA11n	N3	23
OVR A	M5	24
OVRAn	L5	25
DACLK	H2	26
DACLKn	H1	27
SINCOUTA	F2	28
SYNCOUTA	F1	29
ADC_1_OUT[29:0]		
DB0	B7	0
DB0n	A7	1
DB1	B6	2
DB1n	A6	3
DB2	B5	4
DB2n	A5	5
DB3	B4	6
DB3n	A4	7
DB4	B3	8
DB4n	A3	9
DB5	B2	10
DB5n	A2	11
DB6	B1	12
DB6n	A1	13
DB7	C2	14
DB7n	C1	15
DB8	C4	16
DB8n	C3	17
DB9	D2	18
DB9n	D1	19
DB10	D4	20
DB10n	D3	21
DB11	E2	22
DB11n	E1	23
OVR B	D5	24
OVRBn	C5	25
DBCLK	G2	26
DBCLKn	G1	27
SINCOUTB	P5	28
SYNCOUTB	N5	29
ADC_2_OUT[29:0]		

ADC\_10\_11  
ADS5407

ADC\_CTRL[5:0]  
ADC\_SYNC[1:0]  
ADC\_CLK[1:0]

