Custom 12-Bit, 500 MHz ADC/Data Processing Module for the KOTO Experiment at J-Parc

Mircea Bogdan, Jean-Francois Genat, Yau Wah
The University of Chicago

Abstract

We present a custom 4-Channel, 12-Bit, 500 MHz ADC/Data Processing Module, designed for the Step1 of the KOTO Experiment at J-Parc, Japan. This 6U VME Board will receive signals from the Beam Hole Photon Veto Detector, and will be one of the several different ADC Modules in the Experiment's Data Acquisition System (DAQ). In KOTO, the main ADC/DAQ system runs at a 125 MHz simultaneous sampling rate, provided by one low jitter 125 MHz system clock. The 500 MHZ ADC Module receives this system clock and multiplies its frequency by four with a local Zero Delay Clock Generator. The four analog input pulses are amplified and passed to the 12-Bit, 500MHz monolithic pipeline ADC chips. After sampling, data are processed locally with a field programmable gate arrays (FPGAs). The module is provided with a pipeline, up to 40us (20,480 samples) long, which stores the acquisitions, awaiting the system Level 1 trigger pulse. After a trigger, data are packed and buffered for readout. The readout can be performed via the VME32/64 backplane, or via the two front panel optical links. Designed specifically for the KOTO Experiment, this module can also be used in many other Physics applications. The board can receive the analog input signals in both single ended or differential modes and it can run with a local oscillator or with input clocks in the range of 32.5MHz to 550MHz. The full design and test results will be described.

Introduction

We present a custom ADC/DAQ Module designed for the Step-1 phase of K0TO, a high energy physics Kaon experiment at the Japan Particle Accelerator Research Complex (J-PARC). This 4-Channel, 500MSPS ADC Board will receive analog signals from the Beam Hole Photon Veto Detector.

Implementation

Figure 1 presents the Schematic of one ADC channel, configured to run at 500MSPS and with an input signal excursion between 0 and -2V. The input channel bandwidth is about 105MHz at -3dB. In this configuration, the analog signal is amplified, offset, and applied to the A/D chip ADS54RF63, by TI. Signal gain, offset, and bandwidth can be adjusted by changing a few passive components. On the same PCB, any channel can be independently stuffed for a differential or for a single-ended input signal. The implementation shown is single-ended, using BNC connectors. The differential configuration uses LEMO connectors (DF4 in Figure 1).

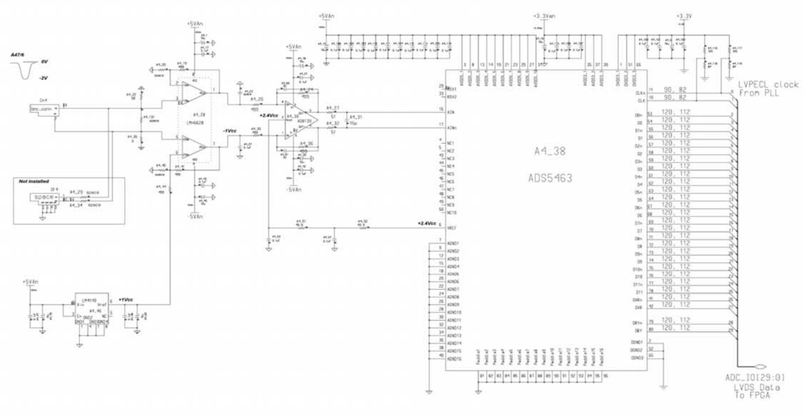


Figure 1: Schematic of one 12-Bit, 500MHz A/D channel. This figure shows the single ended implementation, using one BNC connector per channel. The components marked "'space" are not installed in this configuration. For the differential input signal configuration, connector DF4 (differential LEMO) is used.

Figure 2 presents the block diagram of the ADC Module. In the KOTO Experiment, this module will work on the low jitter, 125MHz system clock. This clock is applied to a Zero Delay PLL Clock Generator ICS8735-21, which provides the 500MHz sampling clocks for the ADC chips. The module can also work with a different input clock in the 31MHz to 700MHz range, as well as with a locally generated clock.

All 4 channels are serviced by one single Field Programmable Gate Array (FPGA), Altera EP2S60F1020C5 chip from the STRATIX II family. The 500 MHz digitized samples are passed to the FPGA, were the data bus is first deserialized and reduced in frequency by a factor of four. All following data processing takes place at the 125MHz system clock frequency.

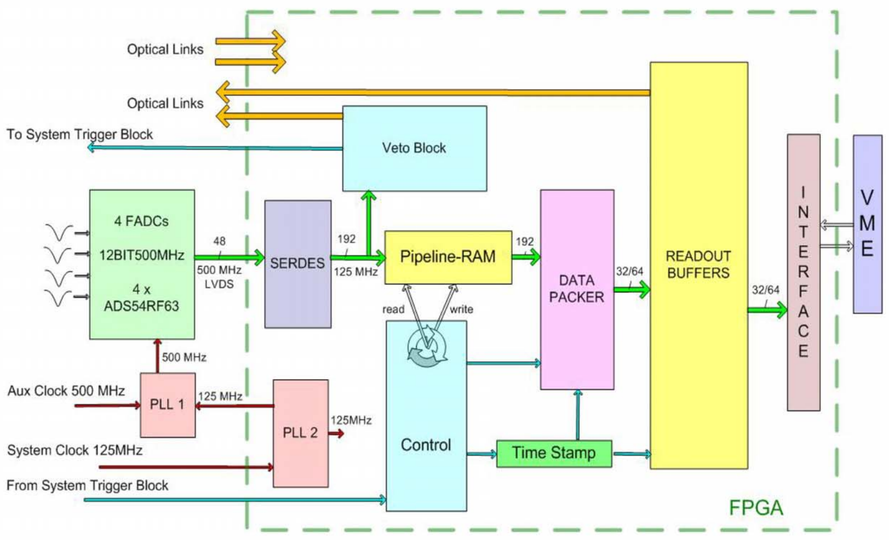


Figure 2: Block Diagram of the 500MHz ADC Module. On single Altera Stratix II FPGA services all 4 ADC channels. 500MHz digitized data are first deserialized and reduced in frequency by a factor of four. All subsequent data processing takes place at the KOTO system frequency of 125MHz.

Beam Hole Photon Veto related values are calculated in real time and sent to the System Trigger block via a front panel Optical Link.

Each ADC module is provided with a pipeline, up to 4us (5,000 samples) long, which stores the acquisitions while awaiting the system trigger pulse. After a trigger, data are packed and buffered for readout. Depending on the volume of data, readout is performed via the 2nd front panel Optical Link, or via the VME64x backplane.

Specifications

Figure 3 present one of the fist prototypes that was build and tested in Chicago. Preliminary test results show an input noise of about 1.3 LSB for a sampling rate of 500MHz, an one-pole input filter at about 110MHz, and a 2Vpp maximum input signal.

ADC Module Specifications:

- 6U VME64x;
- 4 Channel, 12-BIT, up to 550 MSPS ADC:
  - ADS54RF63 by TI;
- Differential /single ended analog inputs;
- Adjustable gain, offset;
- Up to 5,000 sample memory buffer;
- Data readout via VME or optical links;
- Input clock range: 31MHz – 700MHz;
- All I/Os are configurable;
- Front Panel LVDS:
  - RJ45: 3 Inputs, 1 Output;
  - 0.1" Header: 4 Inputs, 4 Outputs;
- Front Panel LVTTL:
  - 8 I/Os configurable;
- Front Panel Optical Links:
  - 2 Inputs 2.5 to 3.125 Gbps;
  - 2 Output 2.5 to 3.125 Gbps;

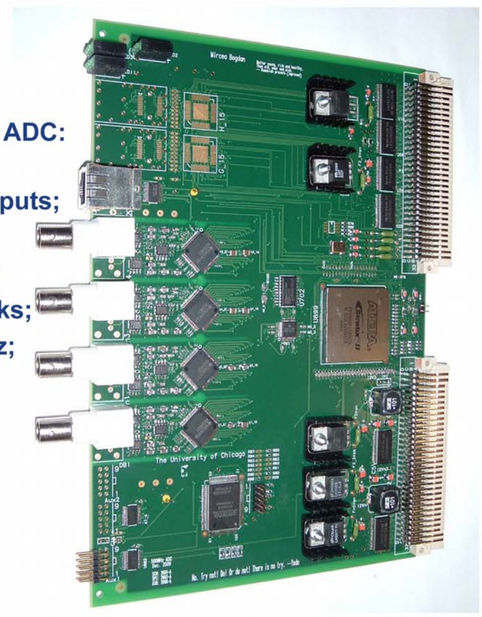
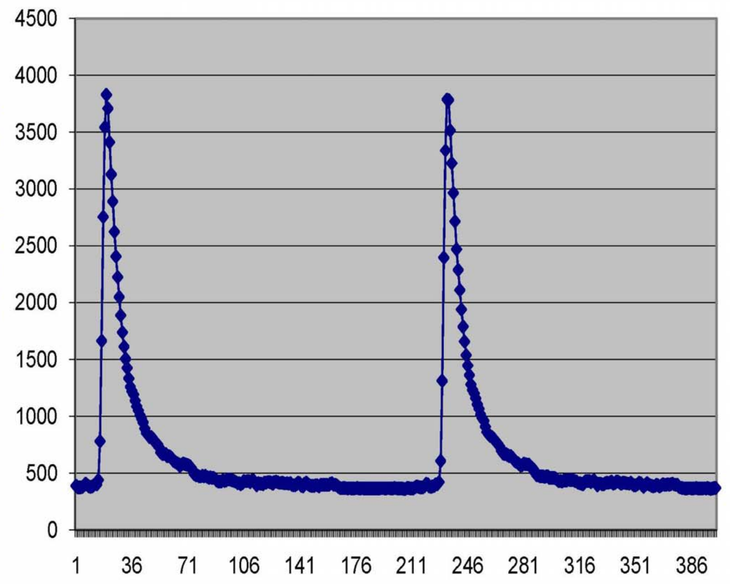


Figure 3: Prototype 4-Channel 500MHz ADC Module. This PCB is stuffed with a single ended input configuration for all channels.

Figure 4:

VME recording of PMT pulses, digitized by the 500MSPS ADC Module.

The original CsI/PMT recorded pulses were normalized and reused as inputs with an Arbitrary Waveform Generator.



Conclusions

Two prototypes 4-channel, 500MSPS, 12-Bit ADC Modules were built so far. They were successfully tested in Chicago, as well as at the April 2010 JPARC-KOTO Beam Test, in Sendai, Japan.

These modules were designed to be used in the KOTO DAQ System, but they also offer a great level of configurability. With minor firmware changes, and/or passive component modifications, these modules can easily be integrated in many other systems, and for many other applications.

The 17th Real Time Conference - RT2010
May 24-28, 2010, Lisbon, Portugal