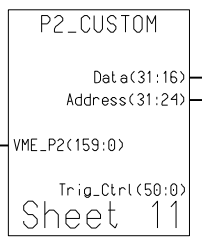
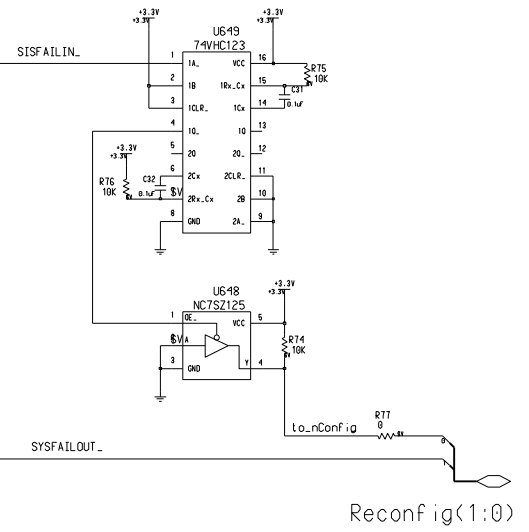
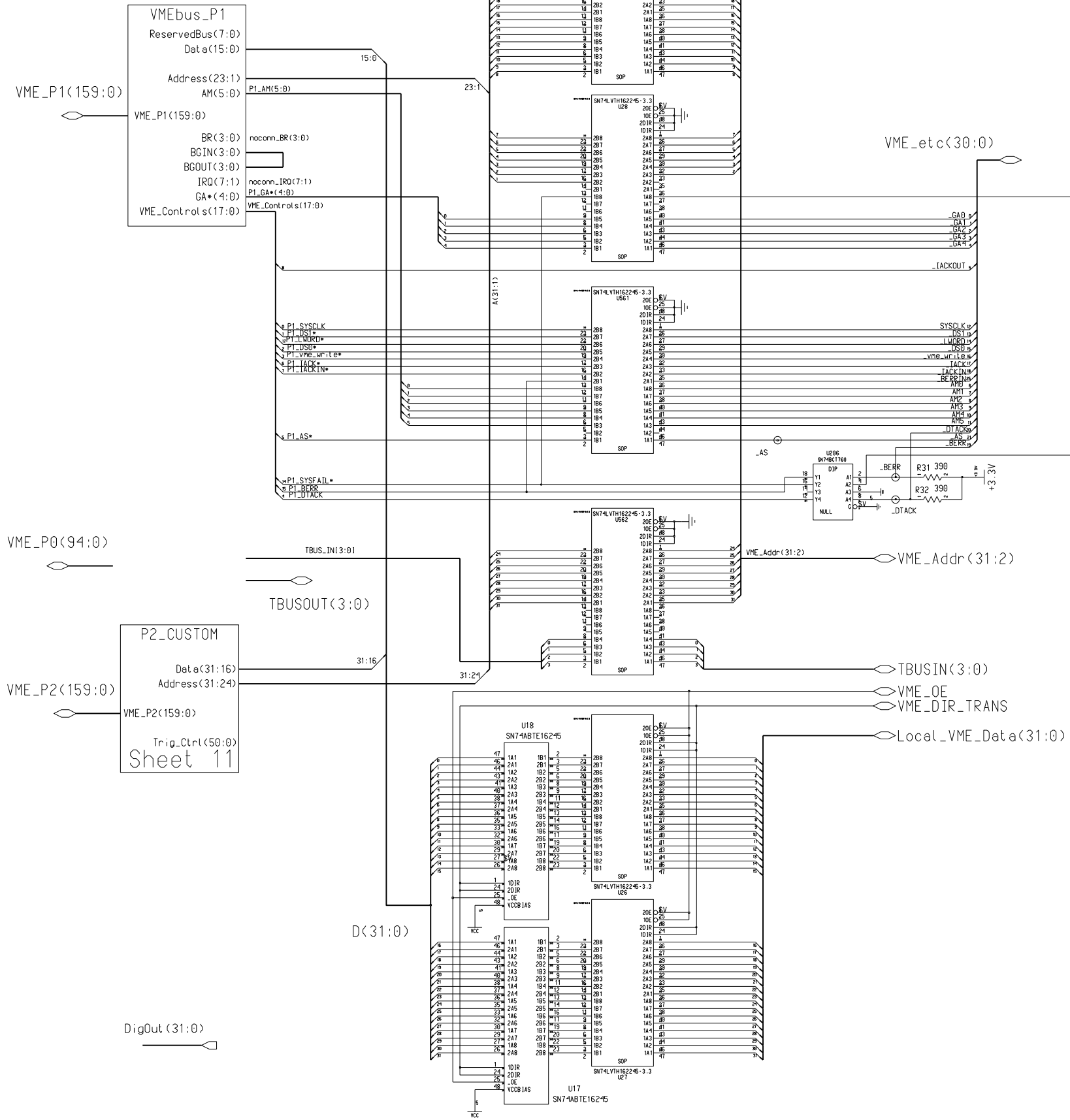


Sheet 9



Engineer	M. Bogdan	The University of Chicago	
Drawn by	M. Bogdan	5640 S. Ellis Ave. Chicago, IL 60637	
R&D CHK		TITLE	Size c
DATE:	11/17/09	VME Interface 500MHz ADC	
TIME:	2:00 pm		
QA CHK		REV	Sheet 8 of 12
		DRW.	2664