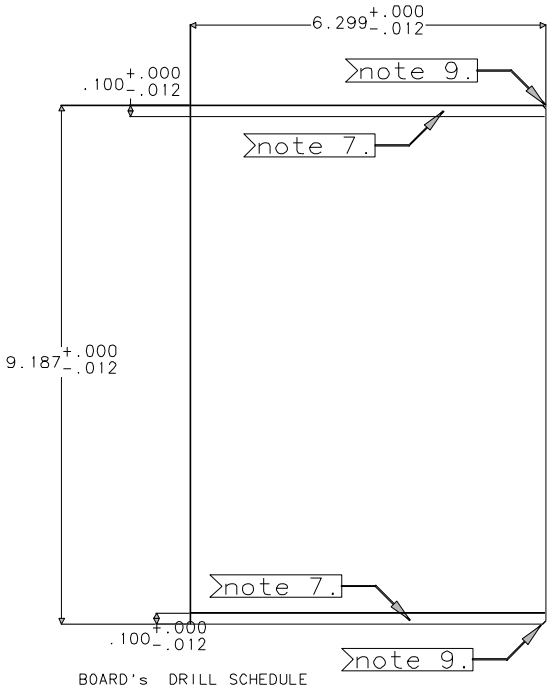

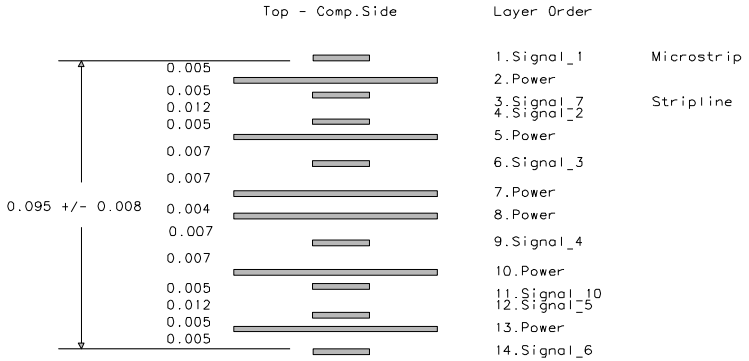

BOARD's DRILL SCHEDULE

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Tolerance	COMMENT
○	.014	1109	YES	---	
⊞	.02	1894	YES	---	
⌀	.035	26	YES	---	
⊟	.037	18	YES	---	
⊖	.041	470	YES	---	
◫	.052	20	YES	---	
⊕	.057	20	YES	---	
□	.062	10	YES	---	
	.106	6	NO	---	
	.12795276	6	YES	---	
	.15	5	NO	---	

Board Characteristics - 14 LAYER BOARD

0. All dimensions are given in inches unless specified otherwise.
1. Material FR4 with Tg>170C, E.g. FR406
2. Minimum trace width: 0.006" and clearence: 0.005" on Signal_1,6 (Top and Bottom);
3. Minimum trace width and clearence: 0.005" on Signal_2,3,4,5,7,8,9,10 (all stripline);
4. 1 oz copper for all power layers and for Signal_1,2 (Top and Bottom)
   1/2 oz copper for Stripline trace layers (Signal_2,3,4,5,7,10).
5. Immersion Gold over copper, with min. Ni: 2.5-5 um; Au: 0.05-0.2 um.
   Apply Solder Mask over bare copper.
6. Board Thickness: 0.093 +/- 0.008
7. Mill the Top and Bottom of board on the solder side to a thickness of 0.063" +/- 0.008
8. Silkscreen on Component and Solder Sides.
9. 45 degree chamfer.
10. FHS tolerances: +/- 0.002 unless specified otherwise.
11. Interlayer spacing as specified.
    Space between Layers 3 and 4, and between Layers 11 and 12, shall be no less than 12mils.
12. Zc=55 Ohm +/- 5 Ohm for 0.005" stripline and 0.006" microstrip traces on all layers.
    Perform TDR test for all signal layers.
    Present TDR test results for all signal layers.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX
.XXX
DO NOT SCALE DRAWING

TREATMENT

FINISH

SIMILAR TO | ACT. WT | CALC WT

CONTRACT NO.

APPROVALS	DATE
DRAWN M.Bogdan	10/10/10
CHECKED M.Bogdan	10/10/10
ISSUED	

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE: 500MHz ADC Board Specification Drawing

SIZE B | FSCM NO. | DWG.NO. 2665 | REV. B

SCALE 1/2 | SHEET

THIS SHEET IS COMPUTER GENERATED