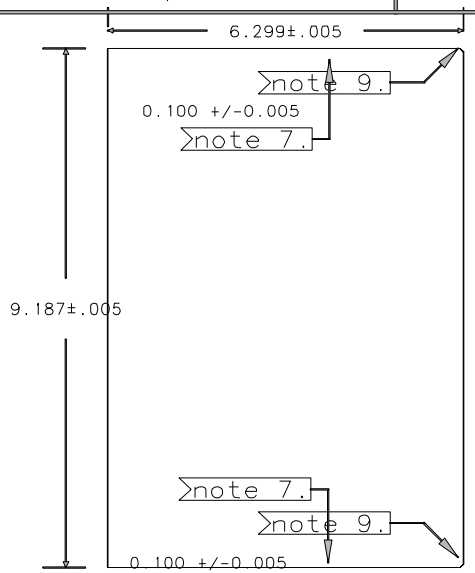
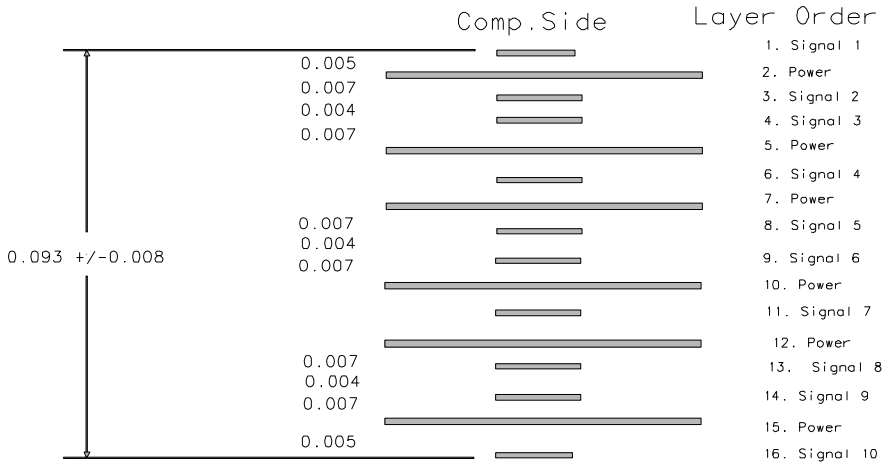
DWG. NO.	SH	REV.
		A





Top_to_Layer_8 Note: Use just one drill size for all blind vias.

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Tolerance	COMMENT
⊞	.0094	368	YES	---	
⊟	.0099	4205	YES	---	

Layer_9_to_Bottom Note: Use just one drill size for all blind vias.

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Tolerance	COMMENT
○	.0092	255	YES	---	
⊕	.0097	4076	YES	---	

Top_to_Bottom

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Tolerance	COMMENT
⊖	.0132	3445	YES	---	
◫	.0133	360	YES	---	
⊕	.014	12	YES	---	
□	.035	1	YES	---	
	.037	9	YES	---	
	.041	678	YES	---	
	.057	40	YES	---	
	.062	2	YES	---	
	.106	6	NO	---	

Board Characteristics

0. All dimensions are given in inches unless specified otherwise.
1. Material FR4 Tg>170C.
2. Minimum trace width 0.005" on all layers.
3. Minimum clearence 0.005" on all layers.
4. 1 oz copper for all traces on top and bottom; 1/2oz on striplines..
5. Ni/Au (chem plated) over bare copper.
   Apply Solder Mask over bare copper.
6. Board Thickness: 0.093 +/- 0.008
7. Mill the Top and Bottom of board on the solder side
   to a thickness of 0.062" +/- 0.008.
8. Silkscreen on Component and Solder Sides.
9. 45 degree chamfer.
10. FHS tolerances: +/- 0.002 unless specified otherwise.
11. Interlayer spacing as specified
13. Impedance : 55 Ohm +/- 5 Ohm for 0.006" traces on all layers.
14. Perform TDR test for preproduction and production first item

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX
.XXX
DO NOT SCALE DRAWING

TREATMENT

FINISH

SIMILAR TO | ACT. WT | CALC WT

CONTRACT NO.

APPROVALS	DATE
DRAWN M.Bogdan	7/28/09
CHECKED M. Bogdan	7/28/09
ISSUED	

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE 1GSPS ADC
Specification Drawing

SIZE	FSCM NO.	DWG. NO.	REV.
B		2645	A

SCALE 1/4 SHEET

THIS SHEET IS COMPUTER GENERATED