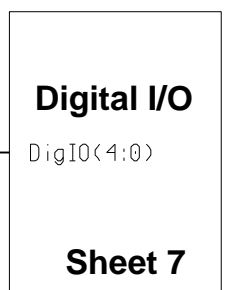


Front Panel

2.5 GBPS →

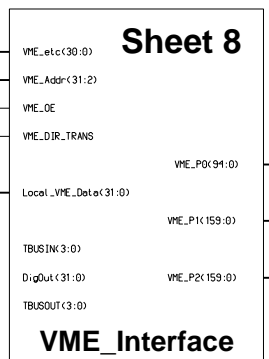
← 2.5 GBPS



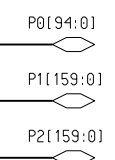
Front Panel

1 Ch LVTTTL →

← 3 Ch LVDS, 1 Ch LVTTTL



VME Backplane



Engineer: M. Bogdan	The University of Chicago <i>5GSPS ADC Module</i> Top Level		
Drawn by: M. Bogdan			
DATE: 7/23/09			
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