Lines common for all 4 DRS4 chips

Independent lines for each DRS4 chip

To Block FPGA
DRS_Control[20:0]

ADC_Control[3:0]

ADC_OUT[21:0]

PDWN
Common to all AD9222

Input A

Input A_

Input B

Input B_

Input C

Input C_

Input D

Input D_

A1_43
DRS4

A1_44
AD9222

Internal Reference Configuration

PIN 0 - Exposed Paddle

Exposed Pad

Ch8_Out[1:0]

Comp_Out[3:0]

DAC[6:0]

Lines common
for all 4 DRS4 chips

Notes:
Each circuit placed on a PCB area of 25mm by 100mm, one side.
4 such circuits on a PCB area of 50mm by 100mm two sides.
4 such circuits are serviced by one local FPGA.

Engineer M.Bogdan		
Drawn by M.Bogdan		
R&D CHK	TITLE	Sampling_ADC Block 1-1
DATE: 7/15/09		*1GSPS ADC Module*
TIME: 11:00 am	REV B	DRW. 2644 Sheet 1_1
QA CHK		