

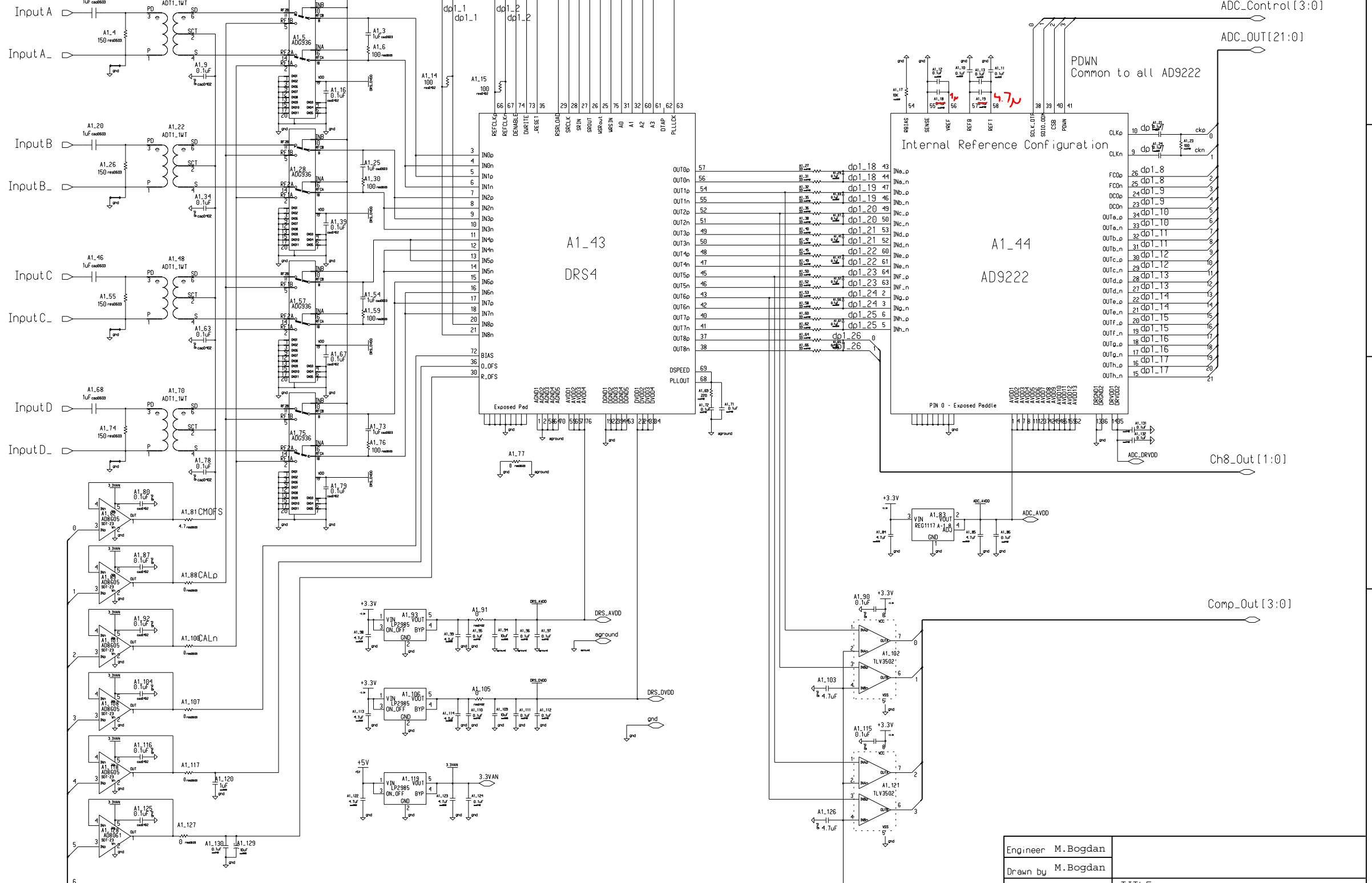
Lines common for all 4 DRS4 chips Independent lines for each DRS4 chip

To Block FPGA
DRS_Control[20:0]

ADC_Control[3:0]

ADC_OUT[21:0]

PDWN
Common to all AD9222



DAC[6:0]
Lines common for all 4 DRS4 chips

Notes:
Each circuit placed on a PCB area of 25mm by 100mm, one side.
4 such circuits on a PCB area of 50mm by 100mm two sides.
4 such circuits are serviced by one local FPGA.

Engineer	M. Bogdan	TITLE
Drawn by	M. Bogdan	
R&D CHK		Sampling_ADC Block 1-1 <i>IGSPS ADC Module</i>
DATE:	7/15/09	
TIME:	11:00 am	
QA CHK		REV B
		DRW. 2644
		Sheet 1_1