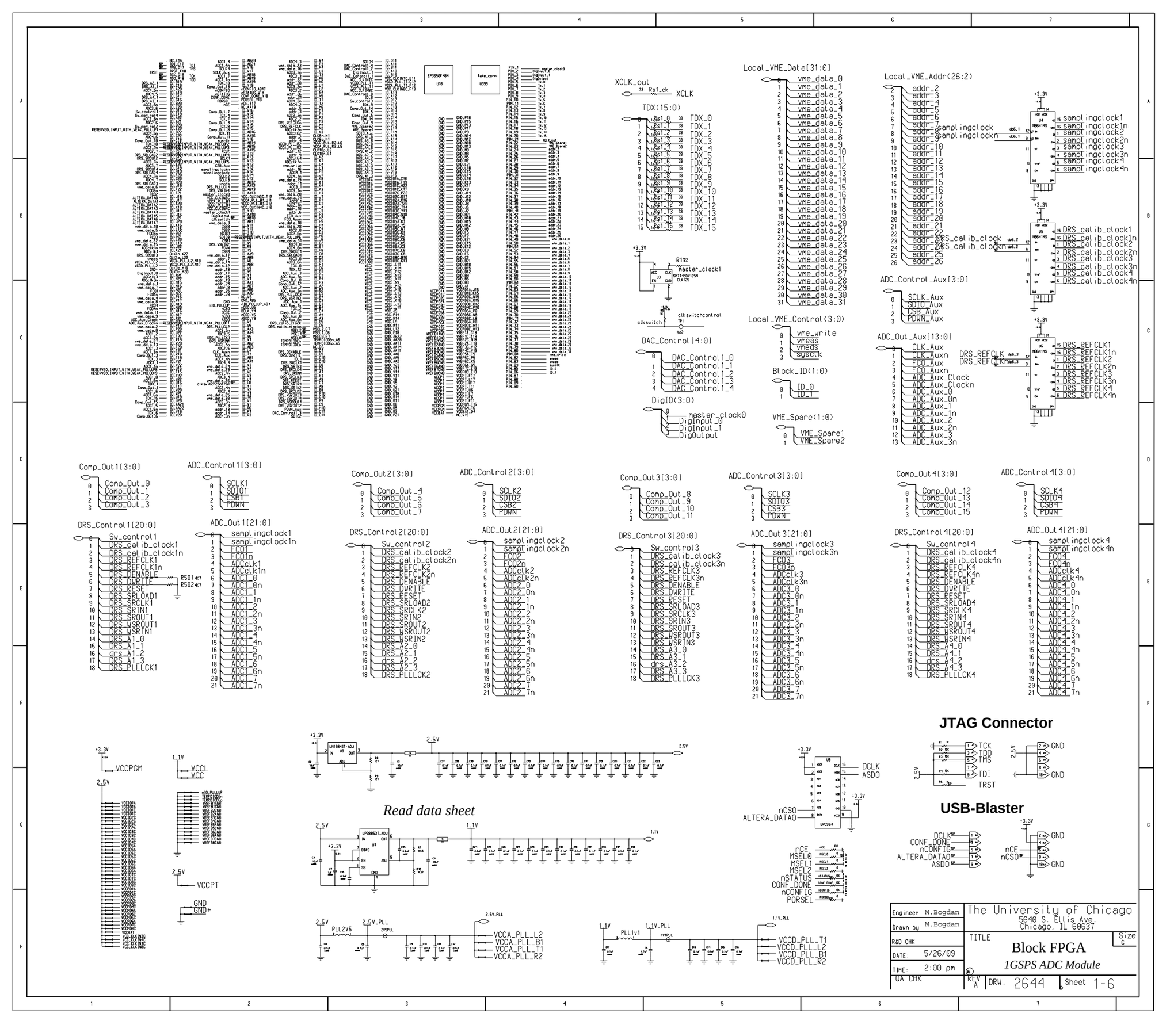
XCLK_out
XCLK
TDX(15:0)
Local_VME_Data[31:0]
Local_VME_Addr(26:2)
ADC_Control_Aux[3:0]
ADC_Out_Aux[13:0]
DAC_Control[4:0]
DigIO(3:0)
Block_ID(1:0)
VME_Spare(1:0)
Local_VME_Control(3:0)
Comp_Out1[3:0]
ADC_Control1[3:0]
DRS_Control1[20:0]
ADC_Out1[21:0]
Comp_Out2[3:0]
ADC_Control2[3:0]
DRS_Control2[20:0]
ADC_Out2[21:0]
Comp_Out3[3:0]
ADC_Control3[3:0]
DRS_Control3[20:0]
ADC_Out3[21:0]
Comp_Out4[3:0]
ADC_Control4[3:0]
DRS_Control4[20:0]
ADC_Out4[21:0]
JTAG Connector
USB-Blaster
Read data sheet
VCCPGM
VCCL
VCC
VCCPT
GND
GND+
2.5V_PLL
PLL2V5
1.1V_PLL
PLL1v1
Engineer M.Bogdan
Drawn by M.Bogdan
R&D CHK
DATE: 5/26/09
TIME: 2:00 pm
QA CHK
The University of Chicago
5640 S. Ellis Ave.
Chicago, IL 60637
TITLE
Block FPGA
1GSPS ADC Module
Size C
REV A
DRW. 2644
Sheet 1-6